1 851 VA-Config Description

2 " " Slot Mount + Rack mount

3 " " Wiring of logic

4 " " Wiring of rack power

5 " " CU-Setup

6 General on Rack Mounting

7

8

9

0

1 CIC - Floppy

2 Floppy Exerciser

3 V24 General

4 P817

5 P851 Panel

6 " BMB + CPU + Pow. Supply

7 " Memory

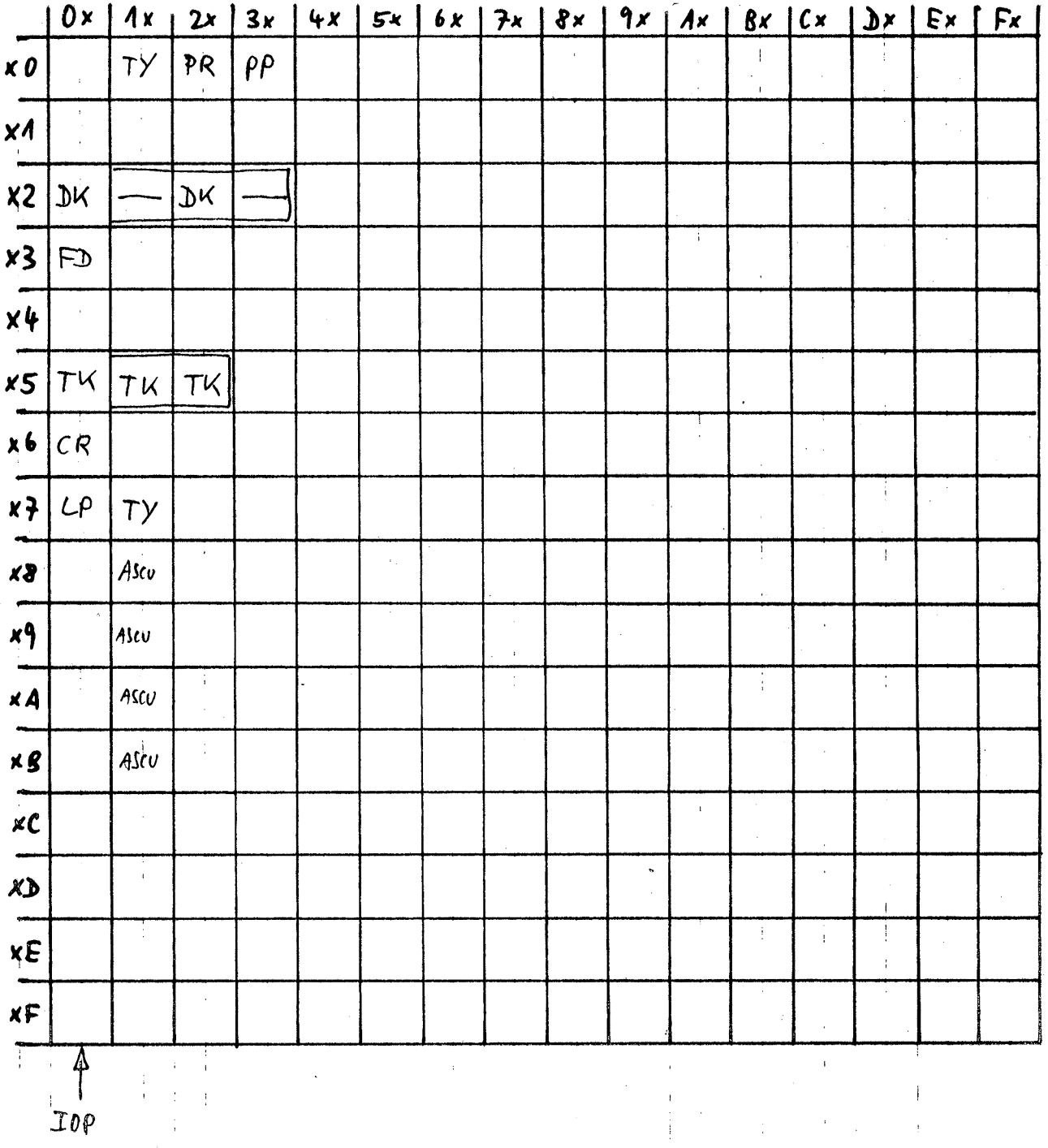
8 div. Items

9 K7 / E2

0 On Bdien - CU's

		GPBS	GPB
0	PWF	–	
1	LUM	–	
2	RTC	–	
3			
4	PR20	1	
5	PP30	Ø	
6	TY10	Ø	
7	CP	1	
8	ASCU	Ø	
9			
A	DK Ø2	–	Ø3
B	TK Ø5	–	Ø4
C	CR Ø6	Ø	Ø5
D	LP Ø7	1	Ø6
E	FD Ø3	–	Ø7
F			

INT. LEVELS


0x 1x 2x 3x 4x 5x 6x 7x 8x 9x Ax Bx Cx Dx Ex Fx
x0 TY PR PP
x1
x2 DK — DK —
x3 FD
x4
x5 TK TK TK
x6 CR
x7 LP TY
x8 Ascu
x9 Ascu
xA ASCU
xB ASCU
xC
xD
xE
xF
IOP
ADDRESS

level				
	0	PWF	–	
	1	LUM	–	
	2	RTC	–	
	3	–		
	4	PR 2Ø	PC	
	5	PP 3Ø	PC	
	6	TY 1Ø	PC	
	7	CP	–	
	8	ASCU 18-19-14-1B	PC	
	9	TY 17	PC	
A	10	DK Ø2-22	MX	
B	11	TK Ø5-15-25	MX	
C	12	(CR Ø6)	(MX)	nicht geplant, CU vorhanden
D	13	LP Ø7	MX	
E	14	(FD Ø3)	(MX)	geplant
F	15	–		

INT. LEVEL

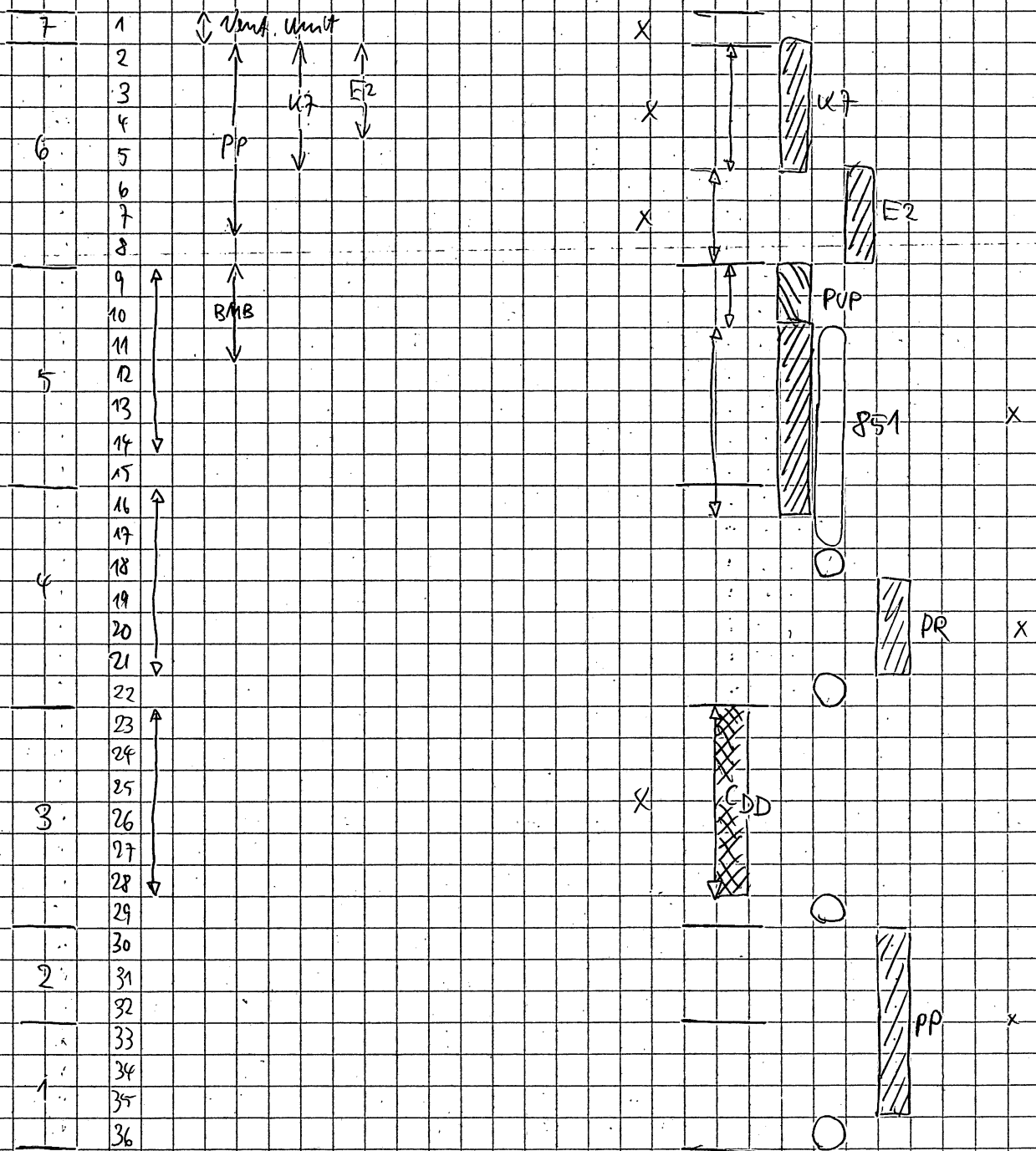
1	CPSZ	
2	IOPZ	
3	GMA1	0..32K
4	SCUZ	AD = /10
5	TRPZ	AD = /20 AD = /30
6		
7	/ASCU4Z	
8	SCUZ	AD = /10
9		
10		
11		
12		
13	IOTZ	

1		
2		
3		
4		AD = /03 | IR = /07
5	MCU2	CR: AD = /06 | IR = /05 || LP: AD = /07 IR = /06
6	CDD	AD = /02 IR = /03

1	K7S2	AD = /05 IR = /04

Slot layout

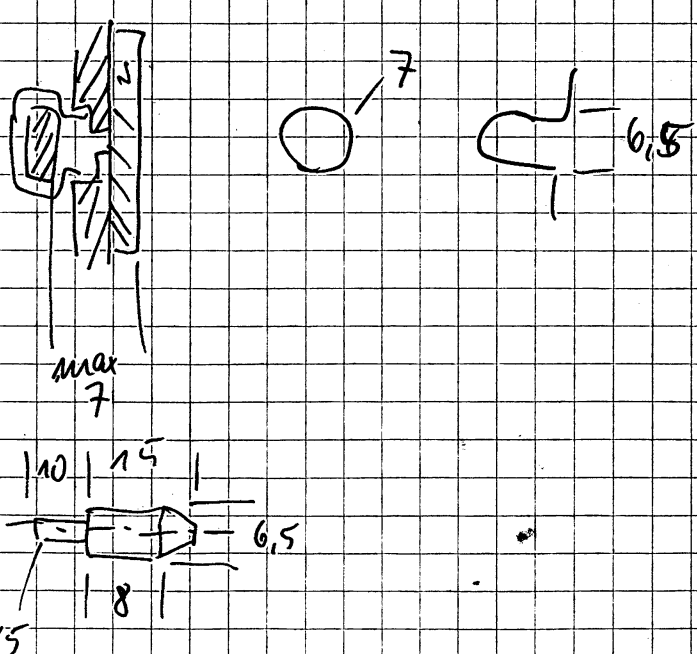
P851/E2/TK


7
6
5
4
3
2
1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
Vent. Unit
PP
U7
E2
BMB
U7
E2
PUP
851
PR
CDD
PP

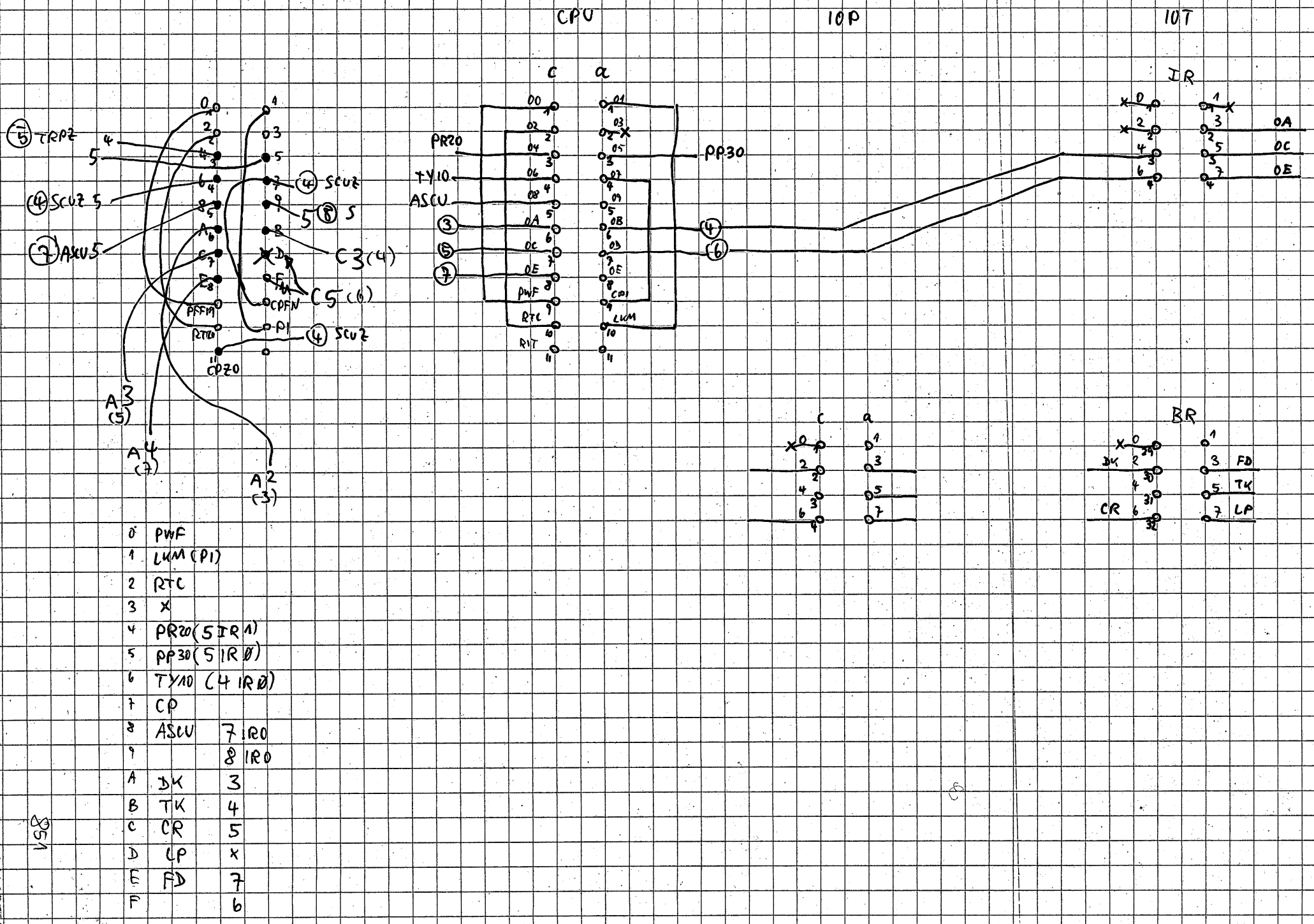
RACK CONFIG

		0	PWF
		1	LUM
		2	RTC
		3	FPP (877)
		4	* PTR 20
		5	* PTP 30
		6	TY 10
		7	CP
		8	
		9	
10		A	DK02
11		B	DK
12		C	DK
13		D	MT 04
14		E	TK 05
15		F	CR 06
16	1	0	PL
17	1	1	LR07
18	1	2	
19	1	3	
20	1	4	
21	1	5	
22	1	6	
23	1	7	
24	1	8	
25	1	9	

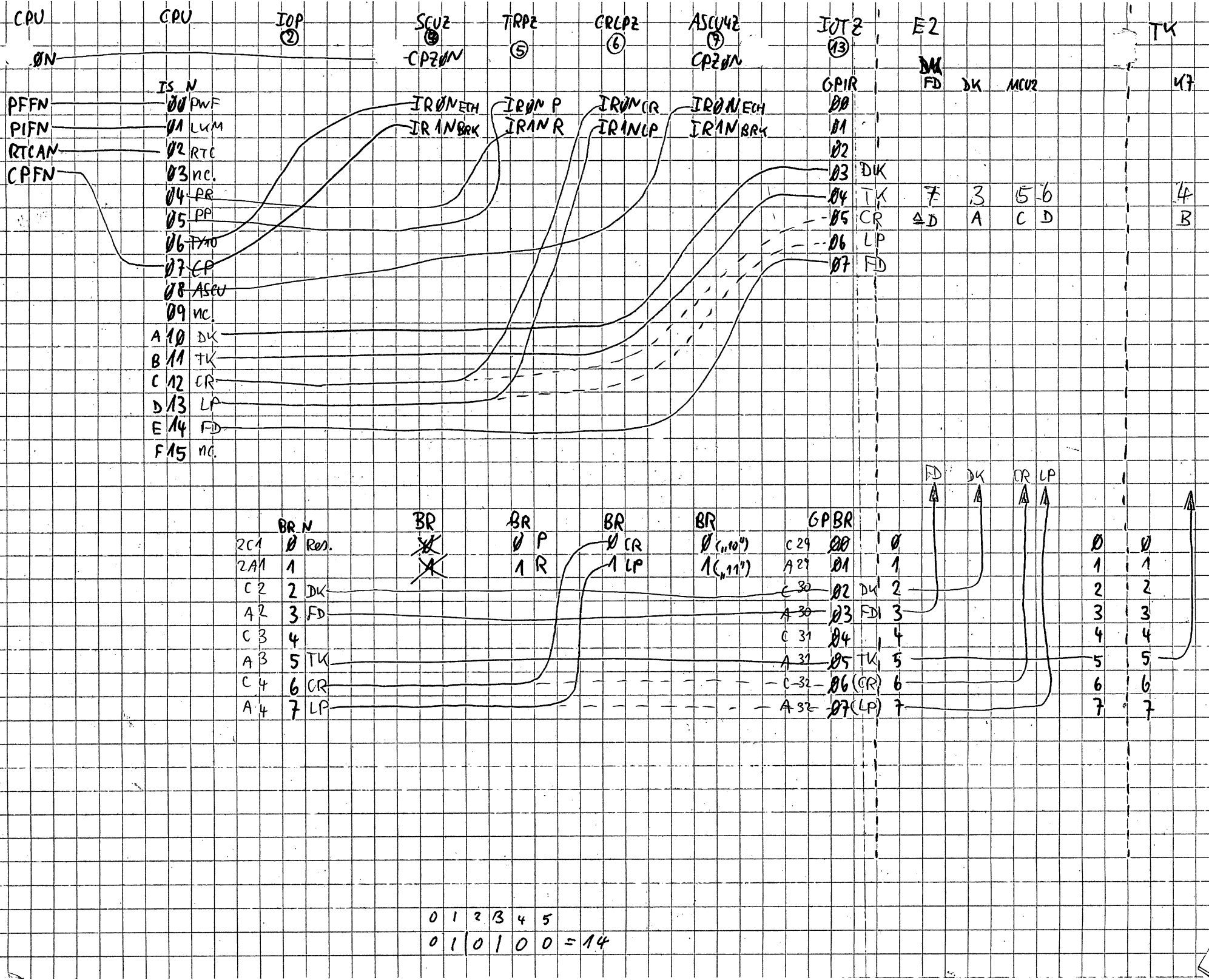
* PTR
DK 01
DK 02
FD
MT
TK
CR
* PTP
LP
DK
DK



F2 · im RACK



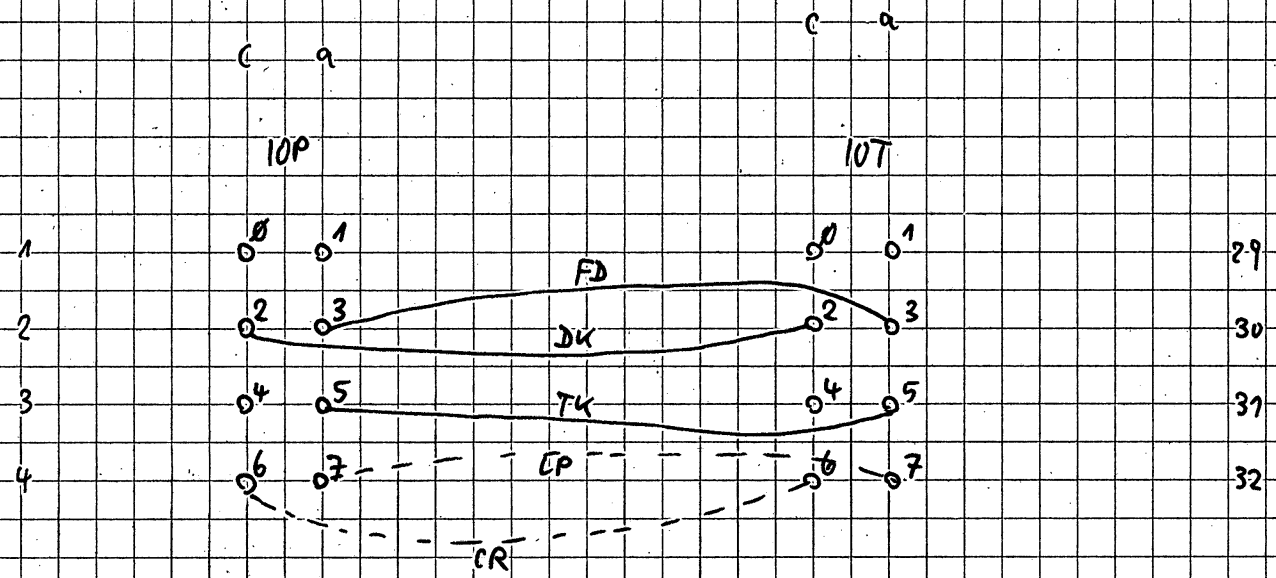
0	PWF	
1	LUM (PI)	
2	RTC	
3	X	
4	PR20 (5 IR 1)	
5	PP30 (5 IR Ø)	
6	TY10 (4 IR Ø)	
7	CP	
8	ASCU	7 IRO
9		8 IRO
A	DK	3
B	TK	4
C	CR	5
D	LP	x
E	FD	7
F		6

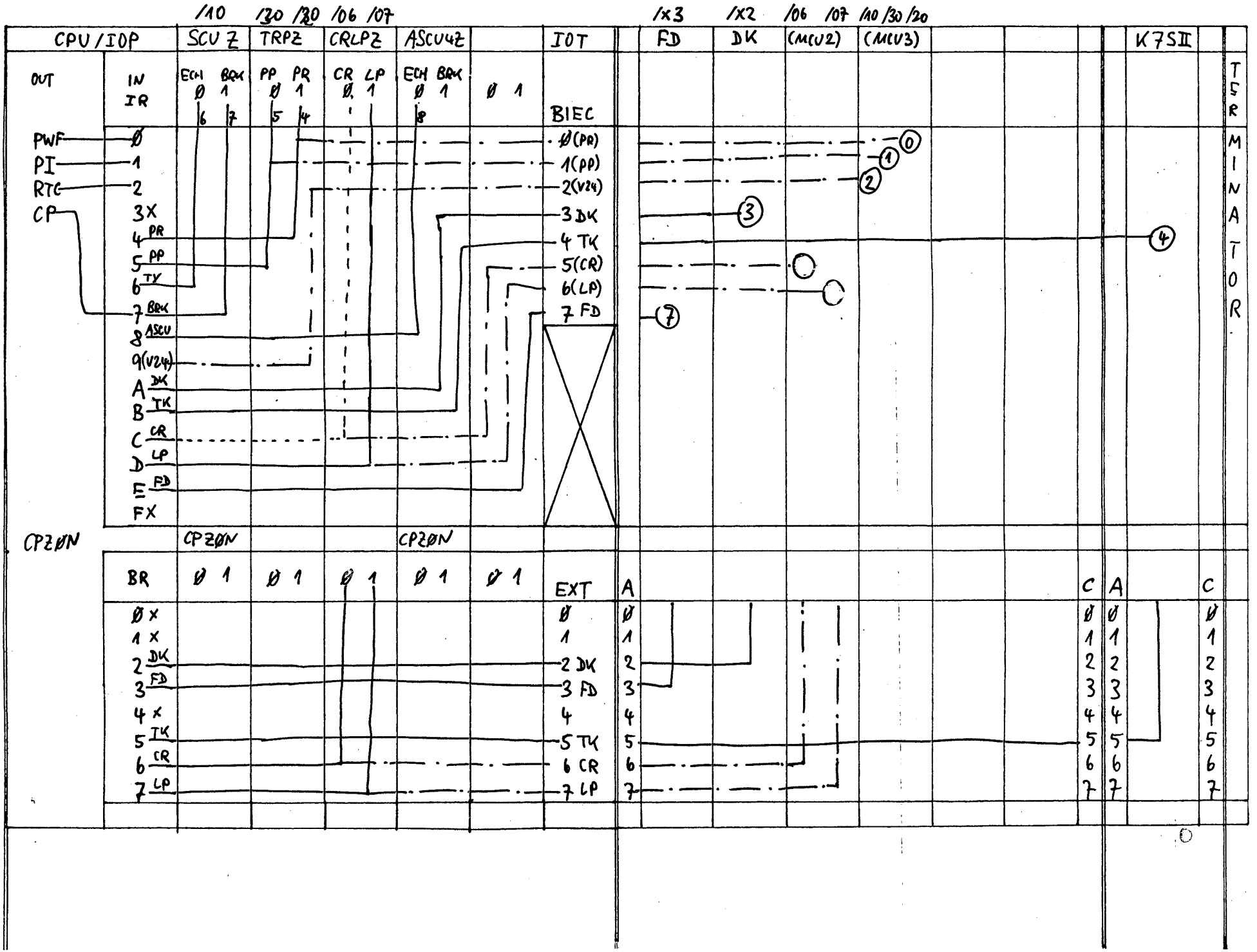

CPU
CPU
IOP ②
SCU2 ③
TRP2 ⑤
CRLP2 ⑥
ASCU42 ⑦
IOT2 ⑬
E2
TK
ØN
CPZØN
CPZØN
IS N
GPIR
FD DK MCU2 47
PFFN
PIFN
RTCAN
CPFN
ØØ PWF
Ø1 LUM
Ø2 RTC
Ø3 nc.
Ø4 PR
Ø5 PP
Ø6 TYØ
Ø7 CP
Ø8 ASCU
Ø9 nc.
A 10 DK
B 11 TK
C 12 CR
D 13 LP
E 14 FD
F 15 nc.
IRØNECH
IR1NBRK
IRØNP
IR1NR
IRØNCR
IR1NLP
IRØNECH
IR1NBRK
Ø3 DK
Ø4 TK
Ø5 CR
Ø6 LP
Ø7 FD
7 3 5 6 4
≙D A C D B
BR N
BR
BR
BR
BR
GP BR
2C1 Ø Res.
2A1 1
C 2 2 DK
A 2 3 FD
C 3 4
A 3 5 TK
C 4 6 CR
A 4 7 LP
Ø P
1 R
Ø CR
1 LP
Ø („10“)
1 („11“)
C 29 ØØ Ø
A 29 Ø1 1
C 30 Ø2 DK 2
A 30 Ø3 FD 3
C 31 Ø4 4
A 31 Ø5 TK 5
C 32 Ø6 (CR) 6
A 32 Ø7 (LP) 7
FD DK CR LP
Ø Ø
1 1
2 2
3 3
4 4
5 5
6 6
7 7
0 1 2 3 4 5
0 1 0 1 0 0 = 14

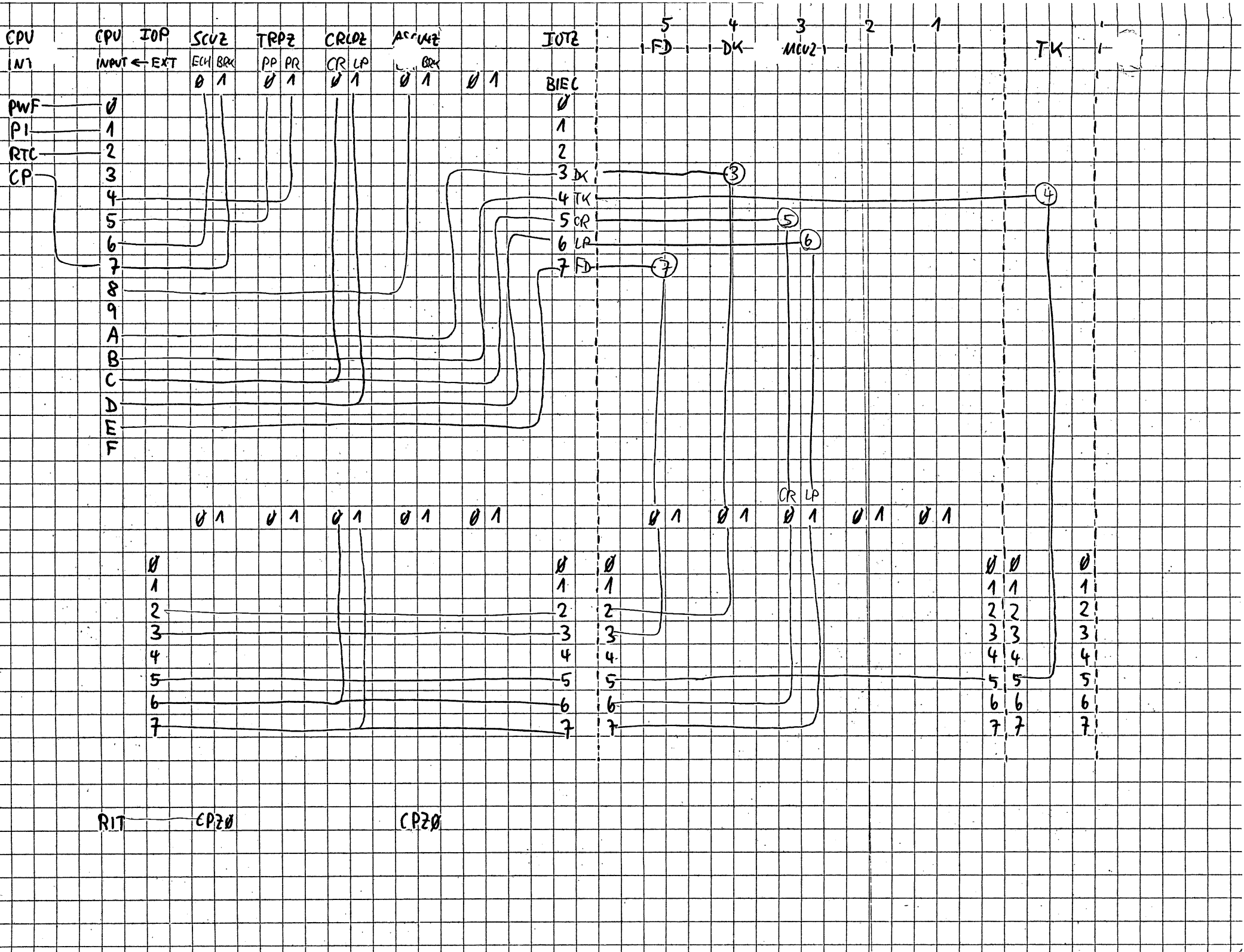
BR

Ø	1	ws
1	2	gn
	3	br
	4	sk
2	5	gr
3	6	bl
	7	rs
	8	re
4	9	sw
5	10	gn-rs
	11	vi
	12	~~ws-gn~~ re-bl
6	13	ws-gn
7	14	ws-sk
		br-gn
		sk-br

BREAK-CABLE


c a
c a
IOP
IOT
1
2
3
4
0 1
2 3
4 5
6 7
0 1
2 3
4 5
6 7
FD
DK
TK
CP
CR
29
30
31
32


/10 /30 /30 /06 /07
/x3 /x2 /06 /07 /10 /30 /20
CPU/IOP
SCU Z
TRPZ
CRLPZ
ASCU4Z
IOT
FD
DK
(MCU2)
(MCU3)
K7SII
TERMINATOR
OUT
IN
IR
ECH BRK
PP PR
CR LP
ECH BRK
BIEC
PWF
PI
RTC
CP
3X
PR
PP
TY
BRK
ASCU
9(V24)
DK
TK
CR
LP
FD
FX
CPZØN
BR
EXT
A
C
Ø(PR)
1(PP)
2(V24)
3 DK
4 TK
5(CR)
6(LP)
7 FD
2 DK
3 FD
5 TK
6 CR
7 LP


CPU IN
CPU INPUT ← EXT
IOP
SCUZ
ECH BRK
TRPZ
PP PR
CRLPZ
CR LP
ASCIIZ
BRK
IOTZ
BIEC
PWF
PI
RTC
CP
DK
TK
CR
LP
FD
5 FD
4 DK
3 MCUZ
2
1
TK
RIT
CPZØ
CPZØ

CPU/IOP							IOT									K7SII		TERMINATOR
OUT	IN IR	Ø 1	Ø 1	Ø 1	Ø 1	Ø 1	BIEC											
PWF	Ø						Ø											
PI	1						1											
RTC	2						2											
CP	3						3											
	4						4											
	5						5											
	6						6											
	7						7											
	8																	
	9																	
	A																	
	B																	
	C																	
	D																	
	E																	
	F																	
CPZØN																		
	BR	Ø 1	Ø 1	Ø 1	Ø 1	Ø 1	EXT	A							C	A		C	
	Ø						Ø	Ø							Ø	Ø		Ø	
	1						1	1							1	1		1	
	2						2	2							2	2		2	
	3						3	3							3	3		3	
	4						4	4							4	4		4	
	5						5	5							5	5		5	
	6						6	6							6	6		6	
	7						7	7							7	7		7	

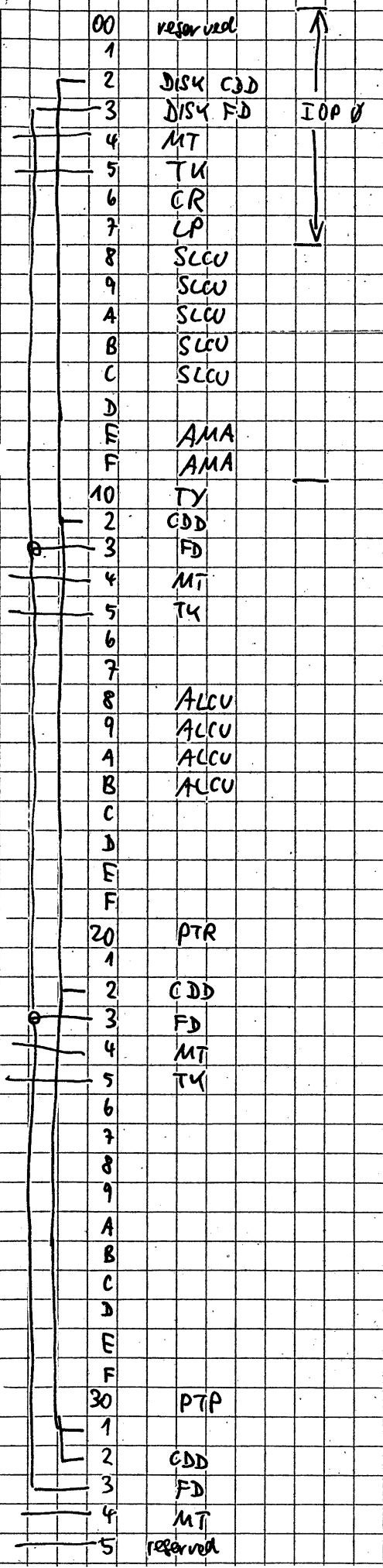
LOC.	LEV.	DEV.	AD.	CHAN.	CU	
00	0	PWF	–	–	–	
02	1	LUM	–	–	–	
04	2	RTC	–	–	–	
06	3					
08	4	PR	20	PC	TRPZ	
0A	5	PP	30	PC	TRPZ	
0C	6	TY	10	PC	SCUZ	
0E	7	CP/BRK		–	–SCUZ	
10	8	[	17.18 19.1A	PC	ASCU4Z]	NOT STD
12	9					
14	A	DK	02-22	MX	CDDB	NOT STD
16	B	TK	05-15-25	MX	K7S2	NOT STD
18	C	[CR	06	MX	CRLPZ]	NO DEVICE
1A	D	LP	07	MX	CRLPZ	
1C	E	[FD	03	MX	FDB]	NO DEVICE
1E	F					

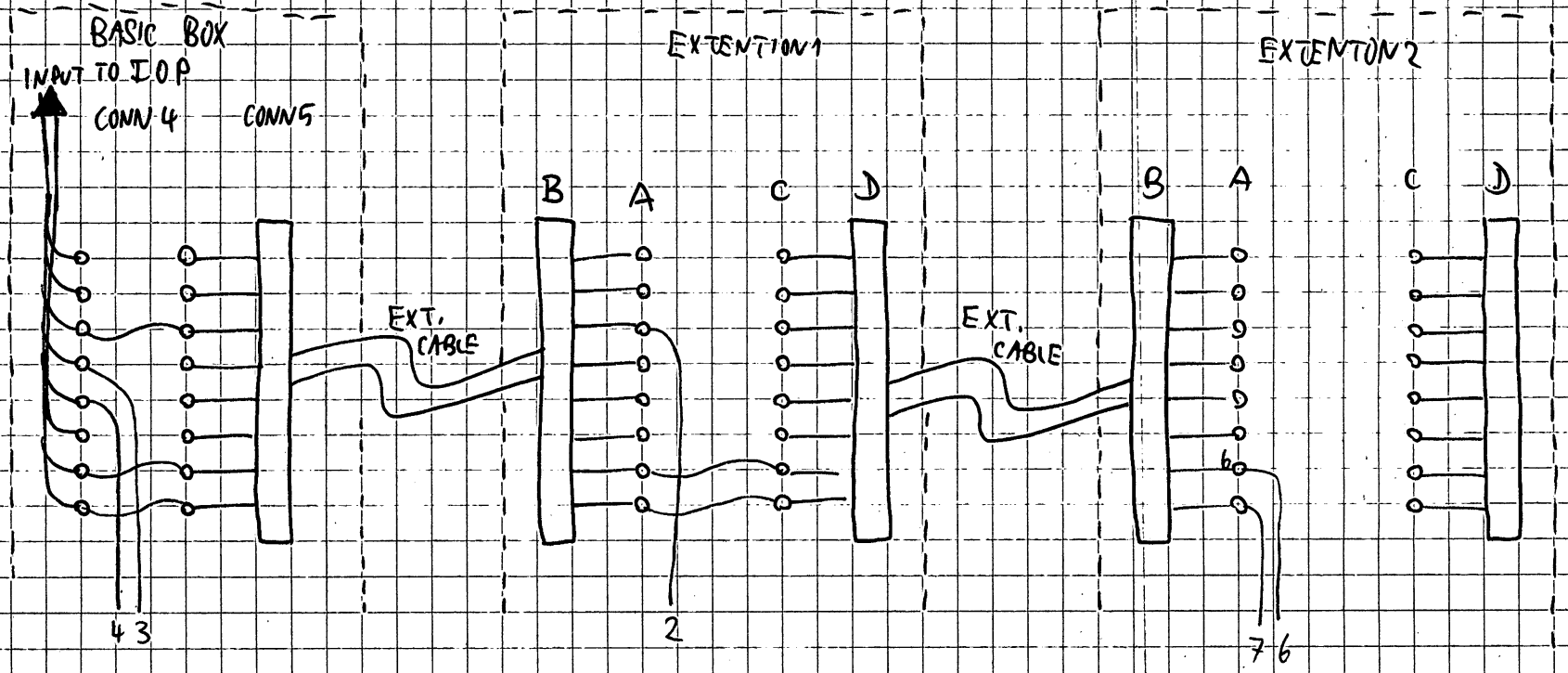
CPU/IOP							IOT									K7SII		TERMINATOR
OUT	IN IR	Ø 1	Ø 1	Ø 1	Ø 1	Ø 1	BIEC											
PWF	Ø						Ø											
PI	1						1											
RTC	2						2											
CP	3						3											
	4						4											
	5						5											
	6						6											
	7						7											
	8																	
	9																	
	A																	
	B																	
	C																	
	D																	
	E																	
	F																	
CPZØN																		
	BR	Ø 1	Ø 1	Ø 1	Ø 1	Ø 1	EXT	A							C	A		C	
	Ø						Ø	Ø							Ø	Ø		Ø	
	1						1	1							1	1		1	
	2						2	2							2	2		2	
	3						3	3							3	3		3	
	4						4	4							4	4		4	
	5						5	5							5	5		5	
	6						6	6							6	6		6	
	7						7	7							7	7		7	

CPU/IOP							IOT									K7SII		
OUT	IN IR	Ø 1	Ø 1	Ø 1	Ø 1	Ø 1	BIEC											TERMINATOR
PWF	Ø						Ø											
PI	1						1											
RTC	2						2											
CP	3						3											
	4						4											
	5						5											
	6						6											
	7						7											
	8																	
	9																	
	A																	
	B																	
	C																	
	D																	
	E																	
	F																	
CPZØN																		
	BR	Ø 1	Ø 1	Ø 1	Ø 1	Ø 1	EXT	A							C	A		C	
	Ø						Ø	Ø							Ø	Ø		Ø	
	1						1	1							1	1		1	
	2						2	2							2	2		2	
	3						3	3							3	3		3	
	4						4	4							4	4		4	
	5						5	5							5	5		5	
	6						6	6							6	6		6	
	7						7	7							7	7		7	

CPU/IOP							IOT									K7SII		
OUT	IN IR	Ø 1	Ø 1	Ø 1	Ø 1	Ø 1	BIEC											TSR
PWF	Ø						Ø											MINATOR
PI	1						1											
RTC	2						2											
CP	3						3											
	4						4											
	5						5											
	6						6											
	7						7											
	8																	
	9																	
	A																	
	B																	
	C																	
	D																	
	E																	
	F																	
CPZØN																		
	BR	Ø 1	Ø 1	Ø 1	Ø 1	Ø 1	EXT	A							C	A		C
	Ø						Ø	Ø							Ø	Ø		Ø
	1						1	1							1	1		1
	2						2	2							2	2		2
	3						3	3							3	3		3
	4						4	4							4	4		4
	5						5	5							5	5		5
	6						6	6							6	6		6
	7						7	7							7	7		7

0	PWF	
1	LKM	
2	RTC	
3		
4	PR	20
5	PP	30
6	TY	10 ~~(11,12,13)~~
7	CPI/BRK	
8		
9		
A	* DK	~~02~~
B	* TK	~~05~~
C	CR	06
D	LP	07
E	FD	~~03~~
F		


00 reserved
1
2 DISK CDD
3 DISK FD
4 MT
5 TK
6 CR
7 LP
8 SLCU
9 SLCU
A SLCU
B SLCU
C SLCU
D
E AMA
F AMA
10 TY
2 CDD
3 FD
4 MT
5 TK
6
7
8 ALCU
9 ALCU
A ALCU
B ALCU
C
D
E
F
20 PTR
1
2 CDD
3 FD
4 MT
5 TK
6
7
8
9
A
B
C
D
E
F
30 PTP
1
2 CDD
3 FD
4 MT
5 reserved
IOP Ø

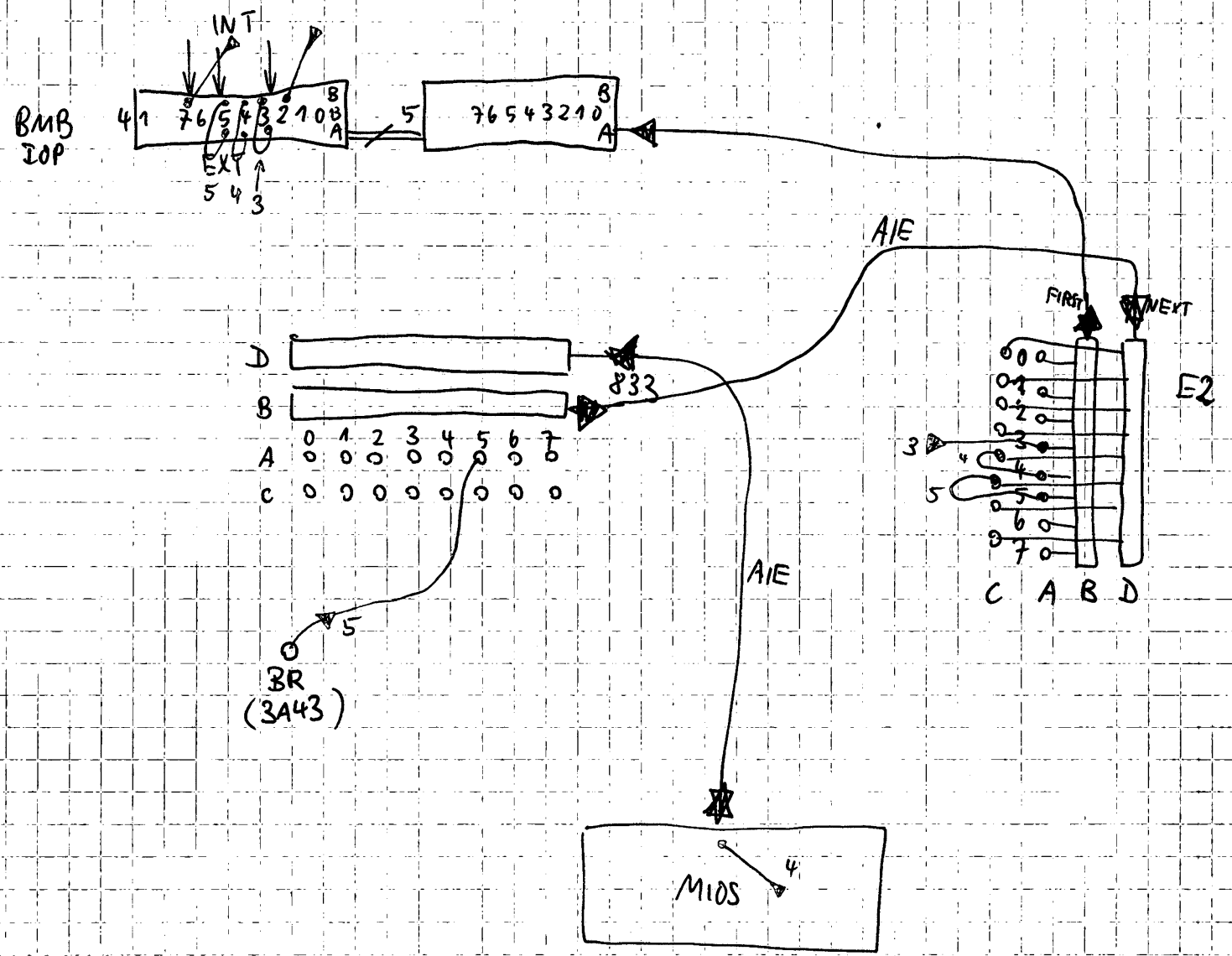


Example channel

	From
0	M.C.
1	M.C.
2	Ext 1
3	Basic
4	Basic
5	M.C.
6	Ext 2
7	Ext 2

BREAK WIRING SYSTEM

BELIER



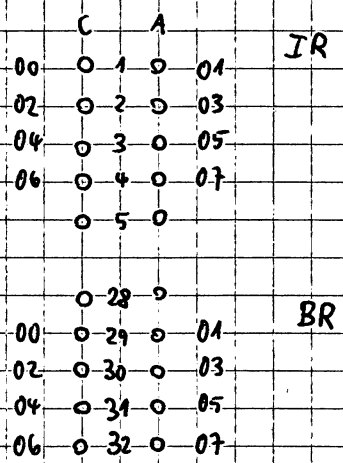
Example:

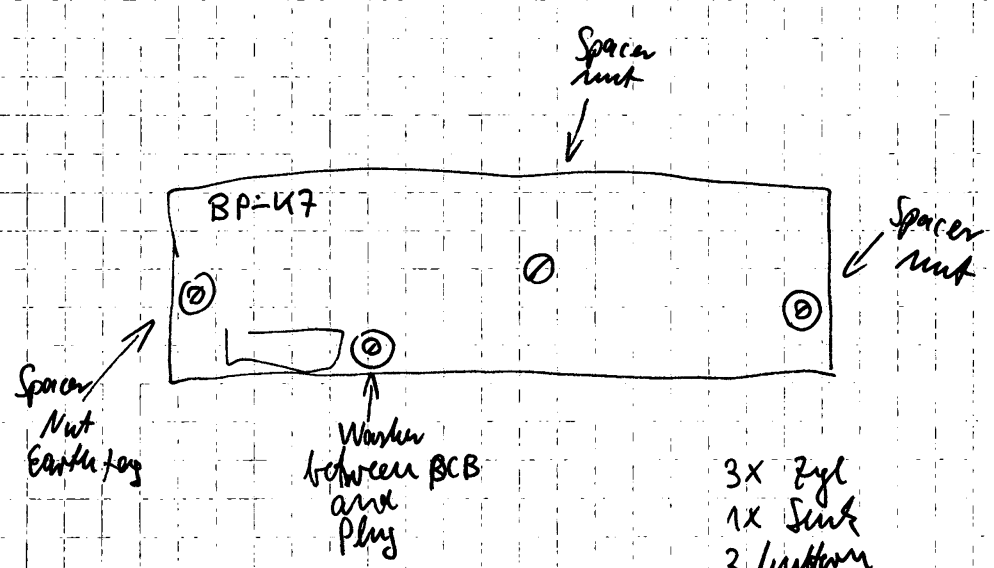
BMB	Channel
E2	2,7
833	3
MIOS	5
	4

∂2

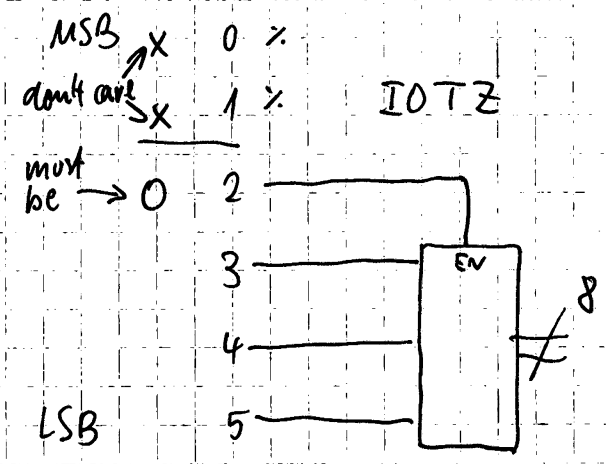
BIEC			BR	
C	1	00	C 29	00
A	1	01	29	01
C	2	02	30	02
A	2	03	30	03
C	3	04	31	04
A	3	05	31	05
C	4	06	32	06
A	4	07	32	07

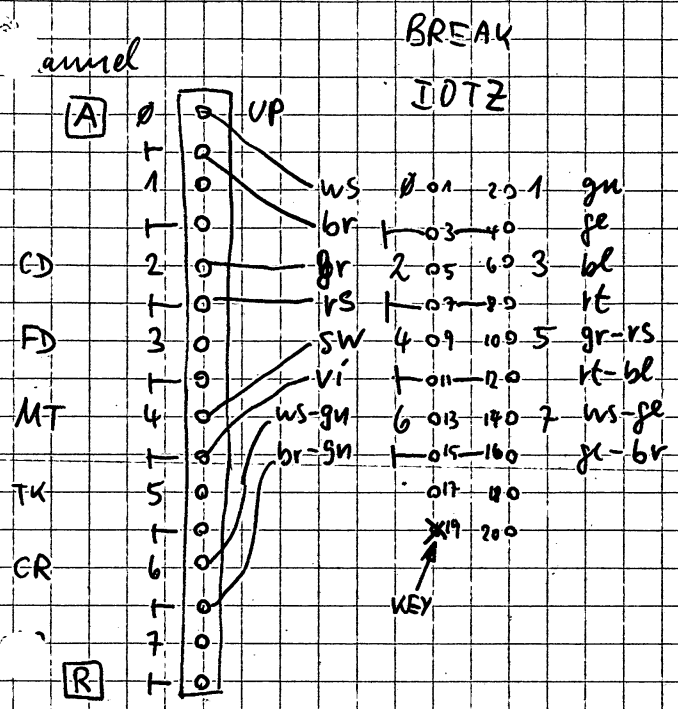
C





3x Zyl
1x Sink
3 Leuchten
4 Iso-Schieben
3 Rollen

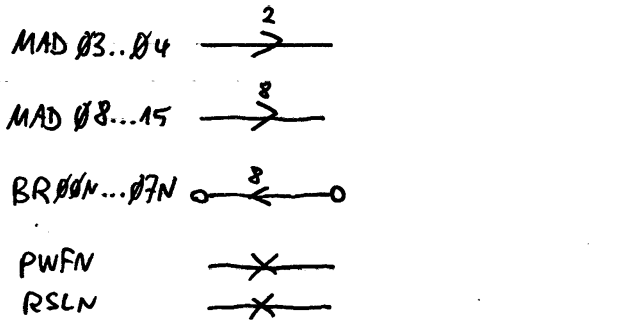


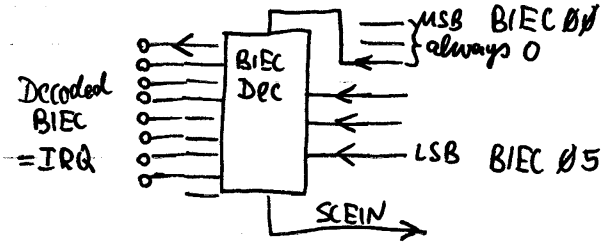


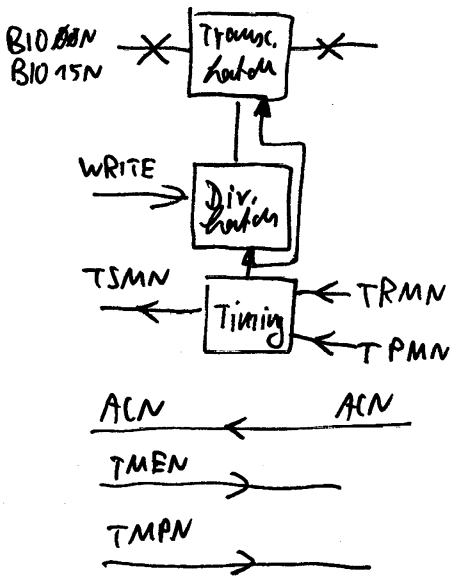
BREAK-CABLE

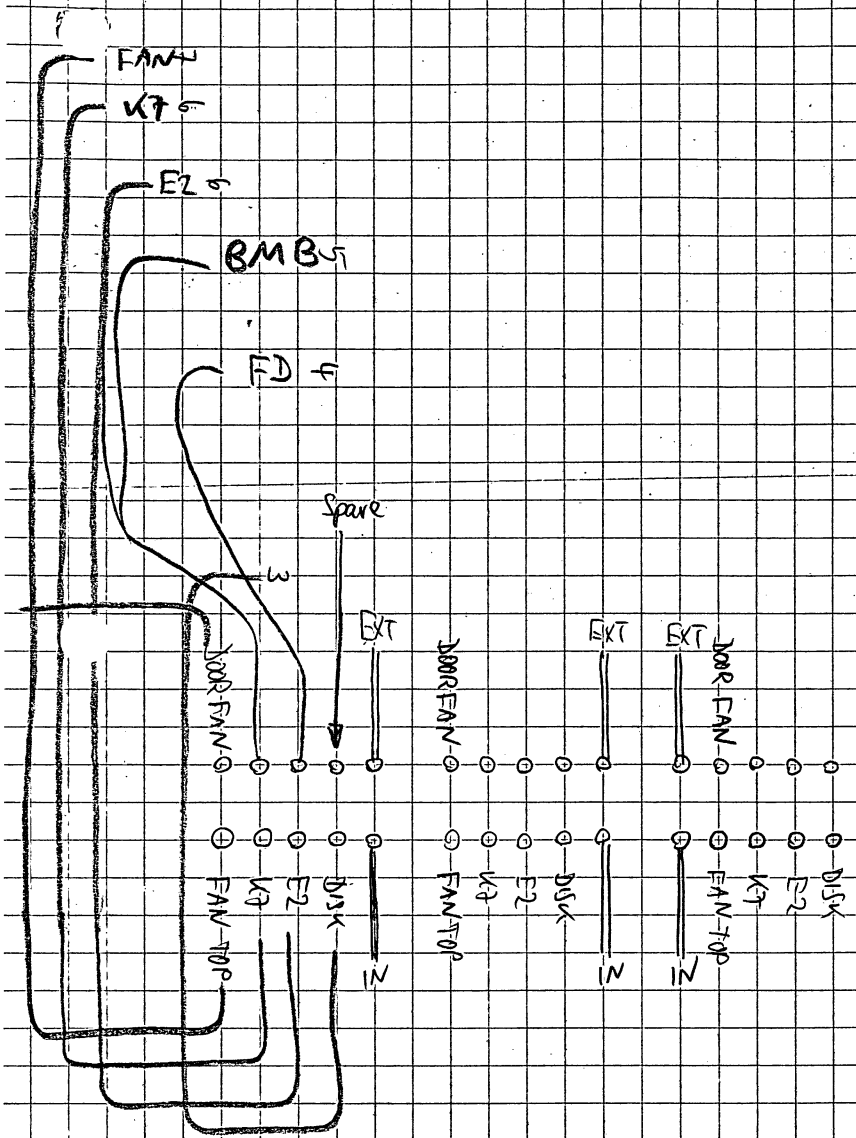
BELIER — IOTZ

P851 GP


MAD Ø3..Ø4
2
MAD Ø8...15
8
BRØØN...Ø7N
8
PWFN
RSLN

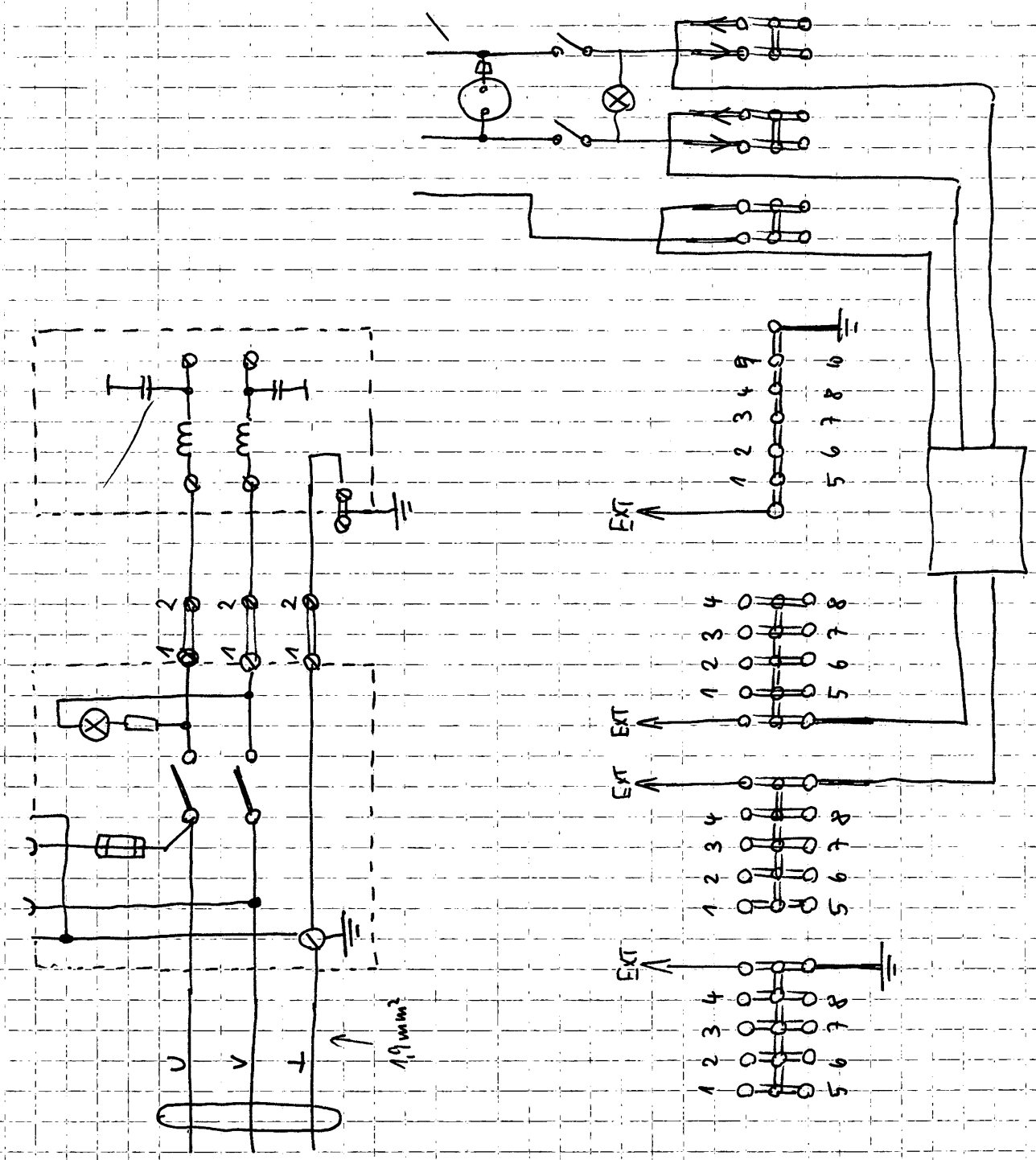

BIEC Dec
Decoded BIEC =IRQ
MSB BIEC ØØ always 0
LSB BIEC Ø5
SCEIN


BIOØØN
BIO15N
Transc. Latch
WRITE
Div. Latch
TSMN
Timing
TRMN
TPMN
ACN
ACN
TMEN
TMPN

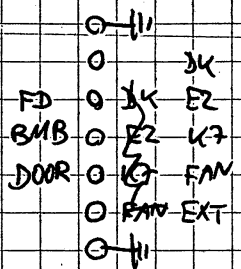


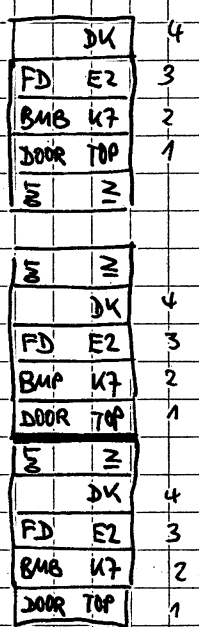
P800 POW. DISTR.

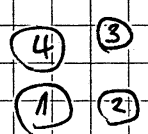
3x5
7



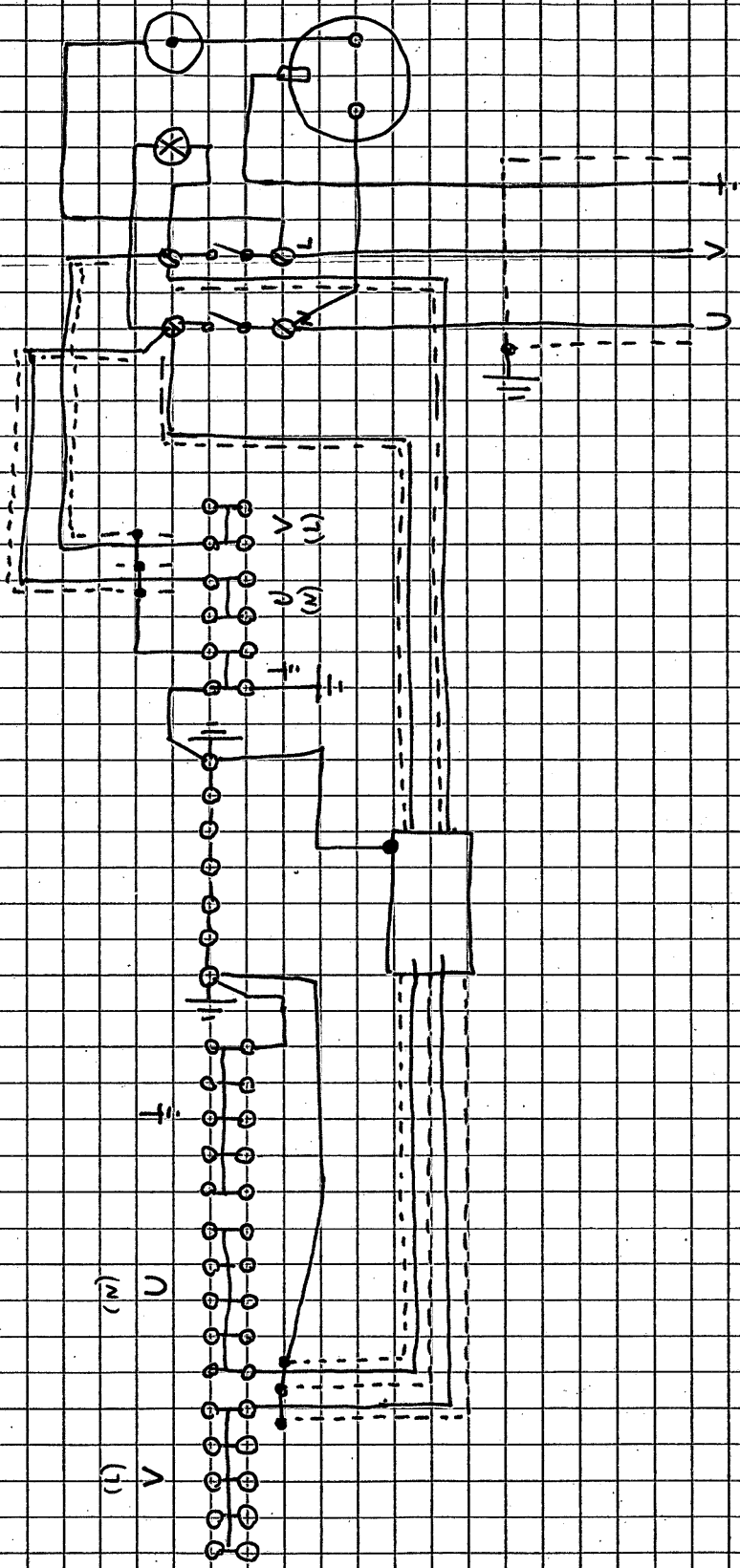
P800 POW. DISTR.

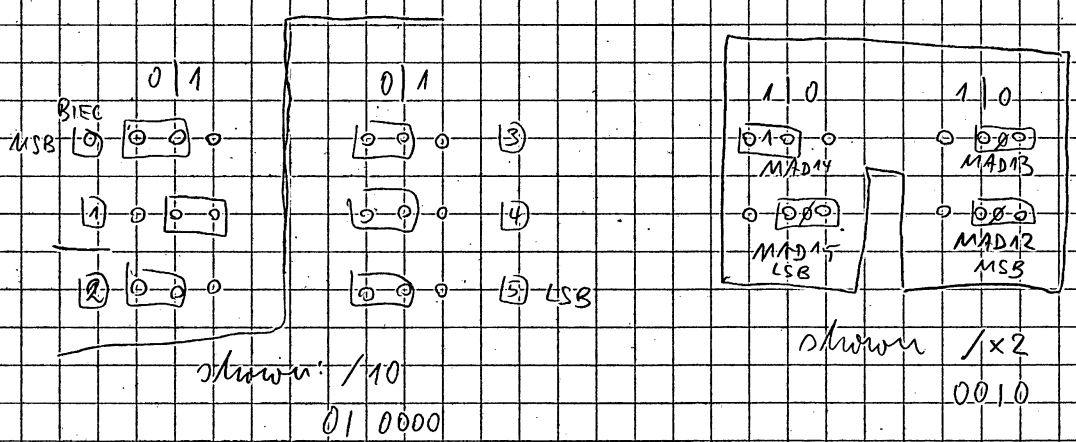






Mains distribution


V (1)
U (2)
U (2)
V (1)



0 = Cantr.
1 = fixed

0 = drive 0 (conn 1)
1 = drive 1 (conn 5)

10	11	12	13	14	15

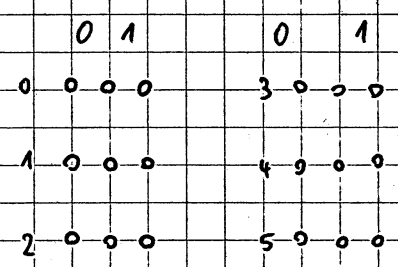
Cantr. decoder.

0	Drive 0	Cantr.
1	Drive 1	Cantr.
2	Drive 0	fixed
3	Drive 1	fixed

CDD

CDD

IR

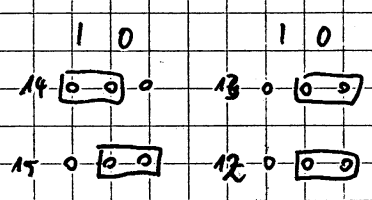


Sfol = /10

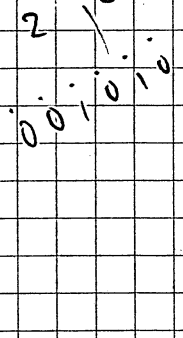
Ø3 =

0	1	2	3	4	5
0	0	0	0	1	1

AD



Sfol = X2 ^{12}0010^{15}



CDD

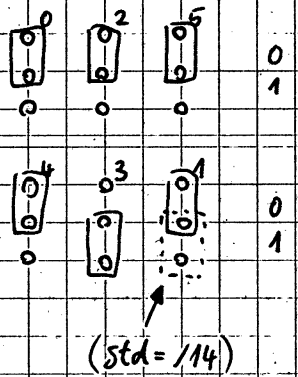
0	1	2	3	4	5
0	0	0	1	0	0

= /04

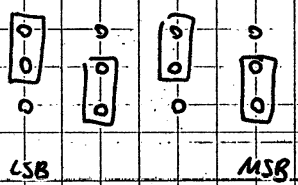
10	11	12	13	14	15
X	X	0	1	0	1

= /x5

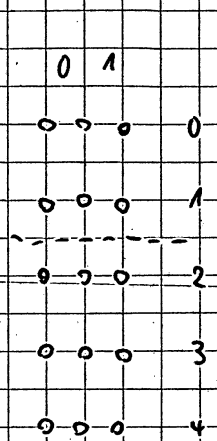
1 0 1 0 = 5 ≙ 05 / 15 / 25

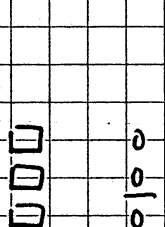


IR



AD

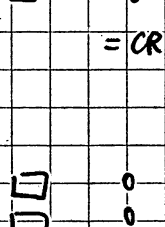




= CR 06

LEV = 05

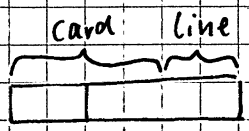
Std. = 0 1 0 1 0 1 = 15



= LP07

LEV = 06

Std = 0 1 0 1 1 1 = 17



P851 IOP

Jumpers				line No 0	1	2	3		
0	0	0	0	00	01	02	03		* AD 100 reserved, other sdol disk
0	0	0	1	04	05	06	07		04=MT, 05=TK, 06=CR, 07=LP; only if none present!
0	0	1	0	08	09	0A	0B		
0	0	1	1	0C	0D	0E	0F		
0	1	0	0	10	11	12	13	not MX IN P 851	11, 12, 13 disk
0	1	0	1	14	15	16	17		14 MT, 15 TK
0	1	1	0	18	19	1A	1B		
0	1	1	1	1C	1D	1E	1F		
1	0	0	0	20	21	22	23		21, 22, 23 disk
1	0	0	1	24	25	26	27		24 MT, 25 TK
1	0	1	0	28	29	2A	2B		
1	0	1	1	2C	2D	2E	2F		
1	1	0	0	30	31	32	33		31, 32, 33 disk
1	1	0	1	34	35	36	37		34 MT
1	1	1	0	38	39	3A	3B		
1	1	1	1	3C	3D	3E	3F		
				PC	PC	PC MX	PC MX		

BRK

ASCU47

1 Paar Teleskope
1 Kabelträger
} Disk

1 Paar Winkel vorn (4 Loch)
1 Paar Winkel hinten (2 Loch)
12 Schrauben 5/32 x 5/16"
8 Käfigmuttern M5 8x8x3
8 Schrauben Zyl. M5 X10
} 19" Rack

2 Träger für 13x13 Rasterloch
2 Schrauben M4x10
2 Muttern M4
} Rack „Euro"

2 Schrauben Rundk. M5 x 12
2 Muttern M5
4 Scheiben M5
} passen nicht, da Bohrungen in Teleskop 4 Stk M4

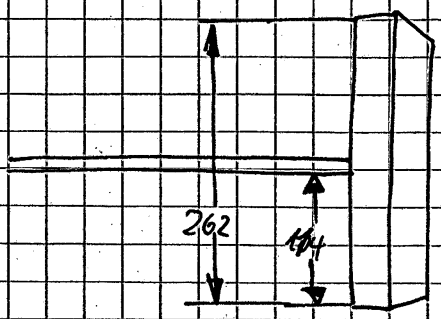
Stattdessen Verwendung
8 Stk Schr. M4x12
8 Stk Federringe
8 Stk gr. Scheiben
8 Stk Mutter M4

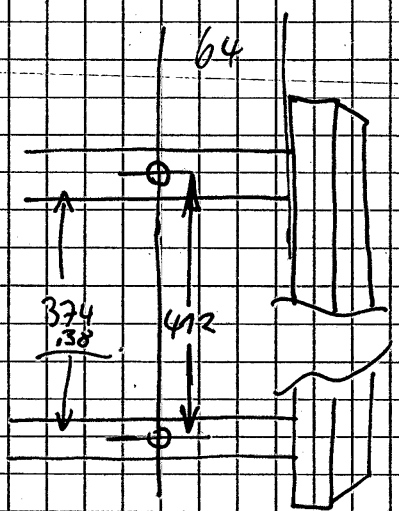
Ergänzungssatz „Ambiance"

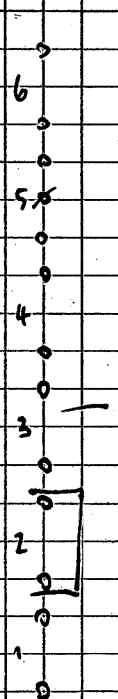
1 Paar Träger für 13x13 Rasterloch
8 Schrauben M4x12
8 Fächerscheiben M4
8 gr. Scheiben M4
8 Muttern M4
4 Schrauben M4 X12
4 Scheiben M4
4 Käfigmuttern M4, 8x8x1
} Kabelträger

2 Spreiznieten
Zusätzlich Verwenden: 8 Käfigmuttern M5 8x8x1

Montagesatz
für X1215/16


262
114

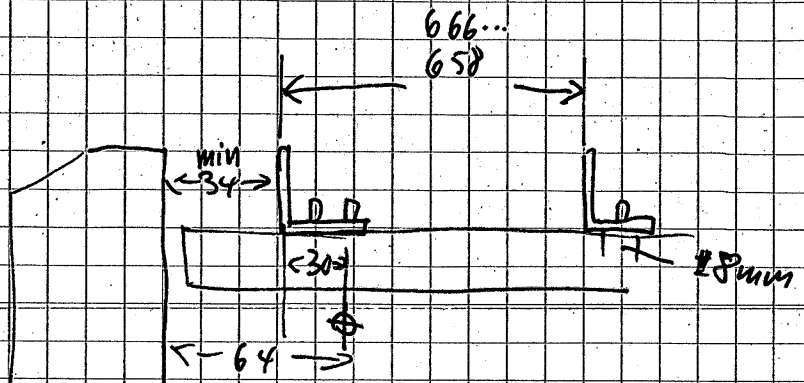

64
374
,38
412

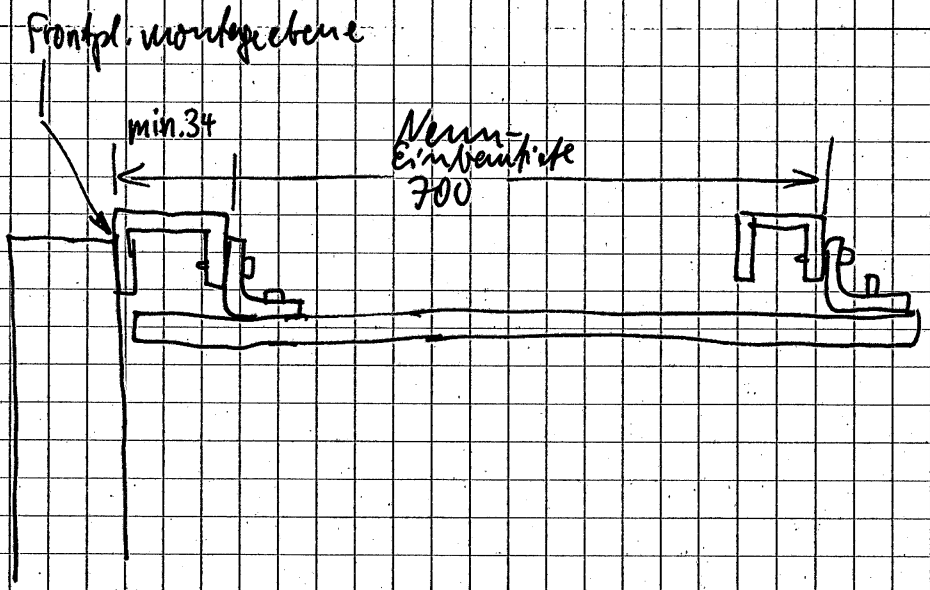

6
5
4
3
2
1

G231

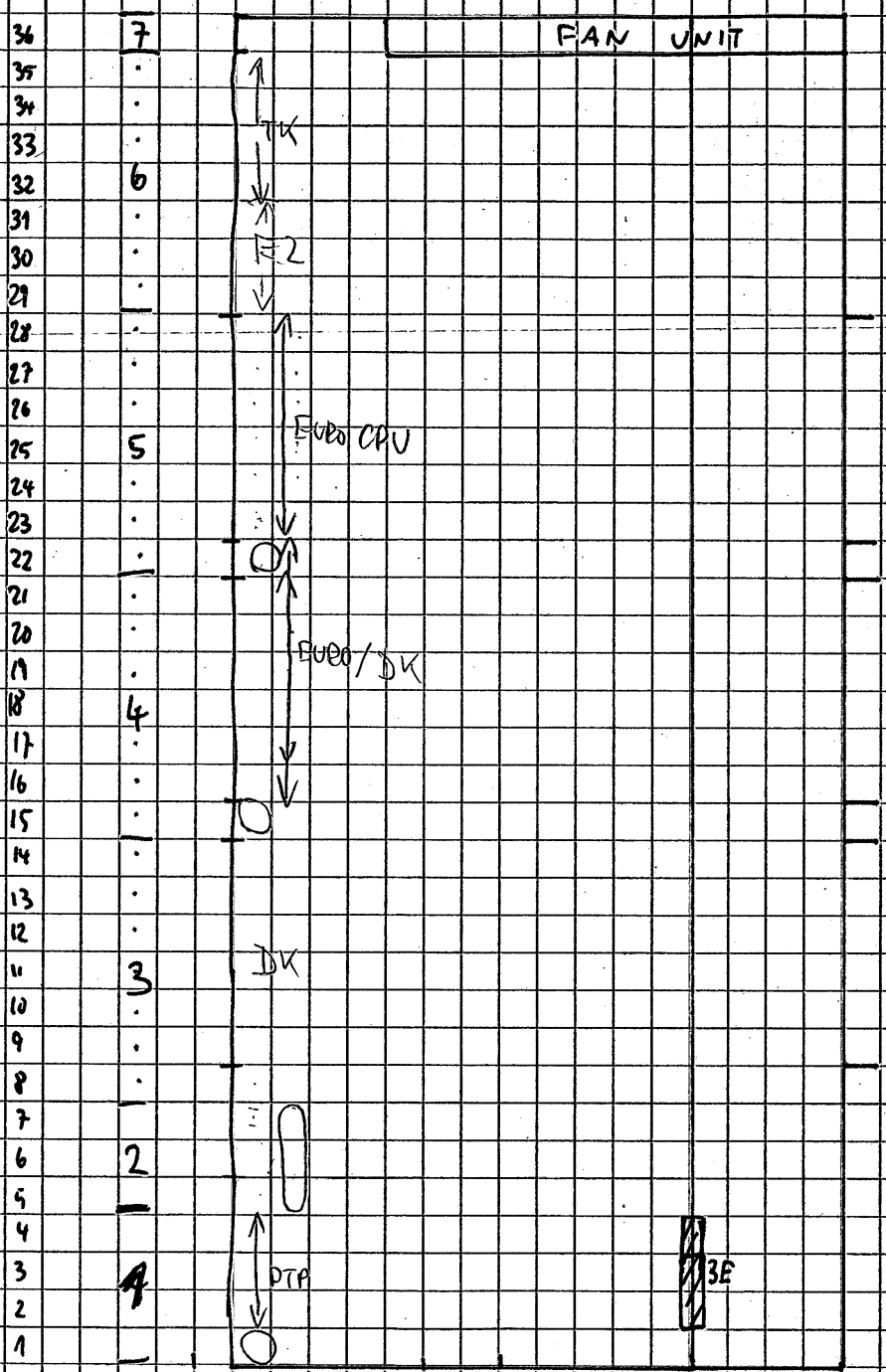
1.2.

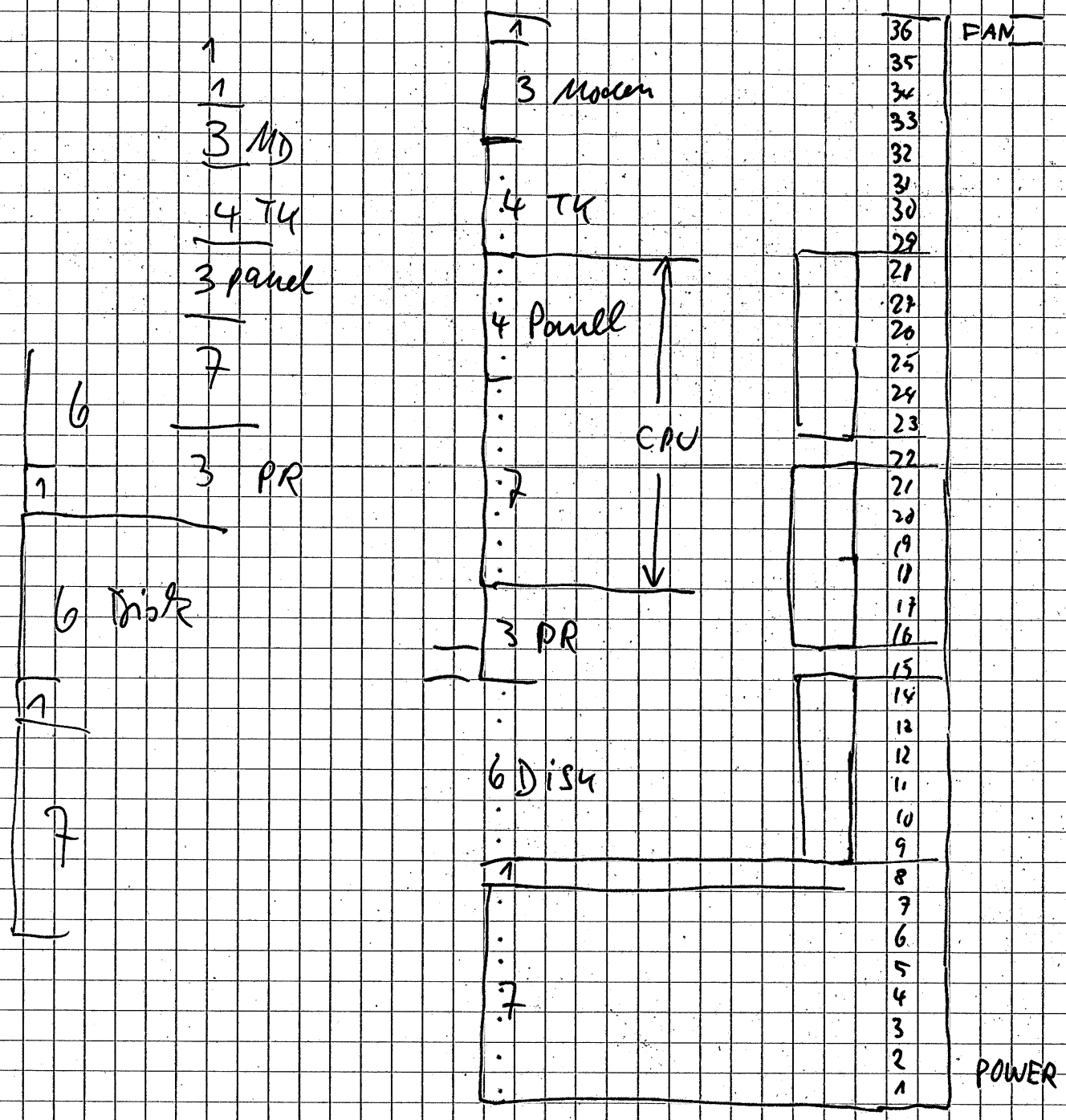
D





X1215


FAN UNIT
TK
E2
EURO CPU
EURO/DK
DK
PTP
3E
7
6
5
4
3
2
1



HE 44,45 = 5 mm

$T_1 = 550$

$T_2 = 700$

2750

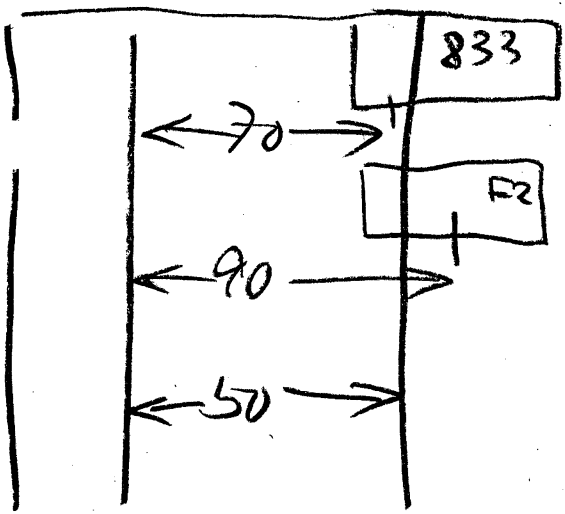
HE : 5 = ~~TE~~ : 550 : TE

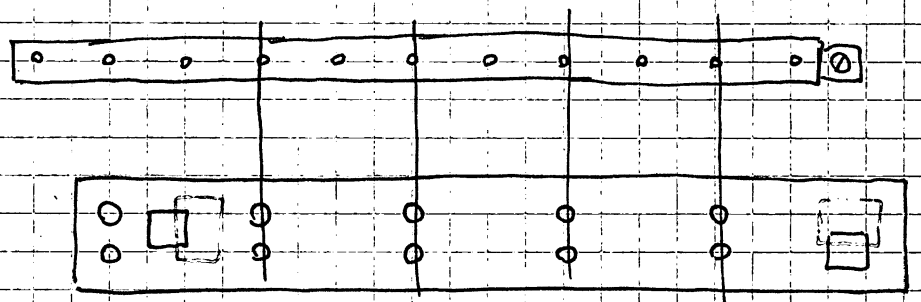
= 700 : TE

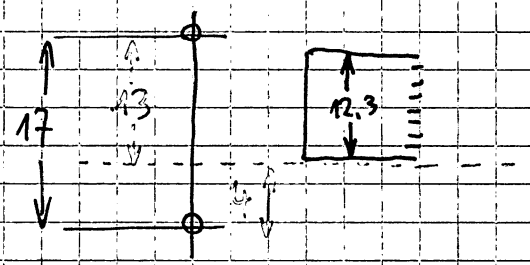
3500

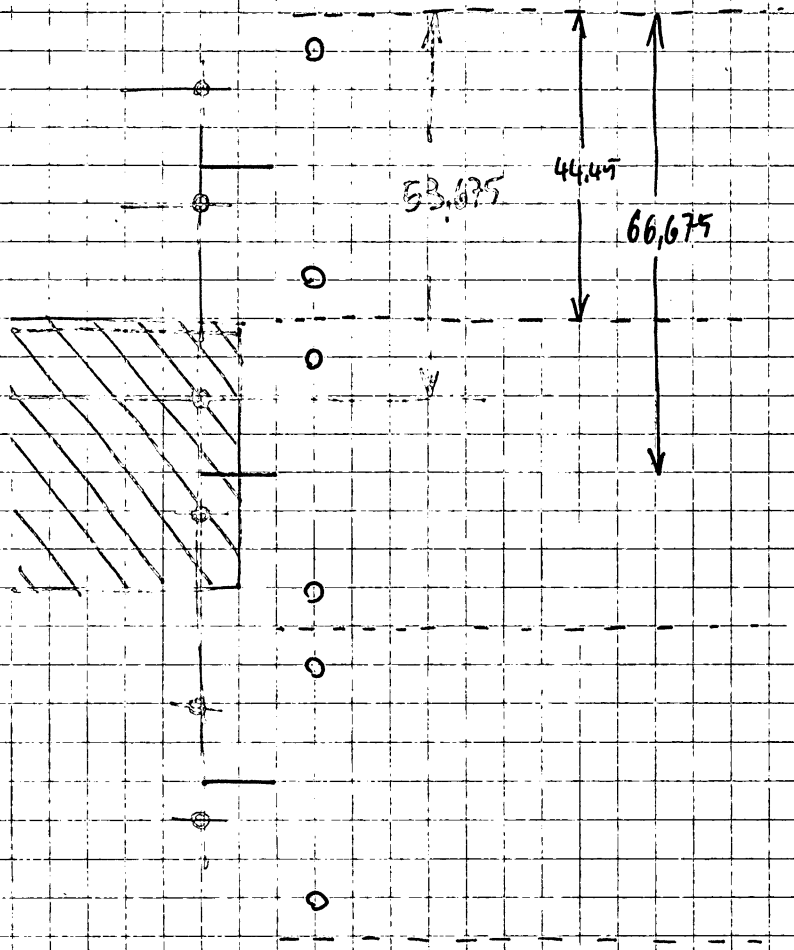
TE = 61,86 ≈ 60

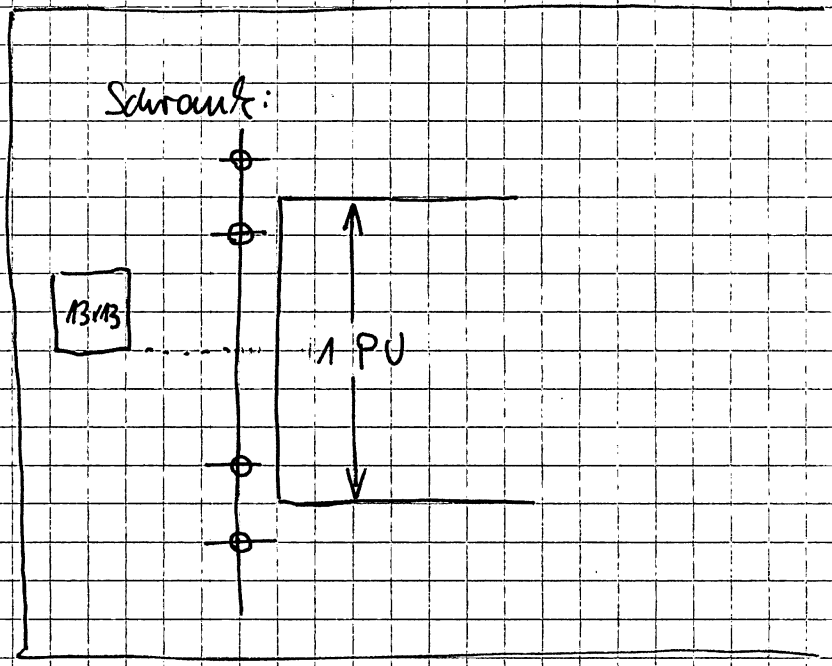
TE = 78,7 ≈ 78


833
70
F2
90
50









D800

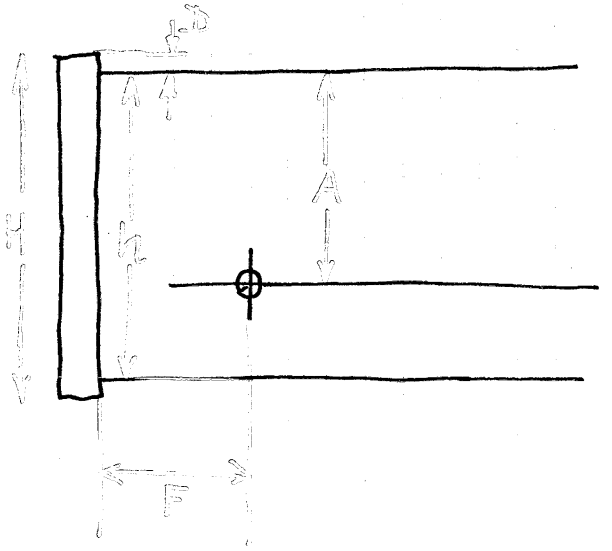
Breite Trag-
schiene

Rechengang

1) nominelle Befestigungsstelle ermitteln

2) Versatz durch Schiene addieren

3) A' damit verpleichen



H Frontplattenhöhe

h Unterschiebe (ohne Schrauben etc)

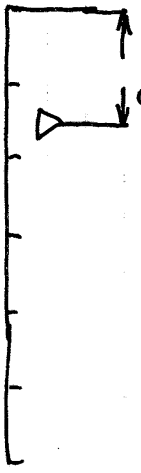
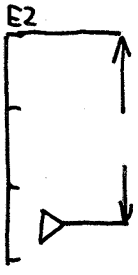
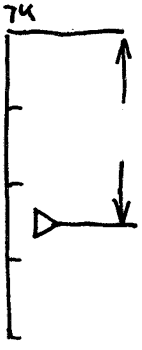
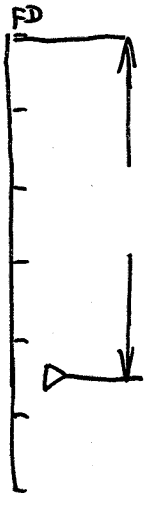
D Differenz an Oberkante

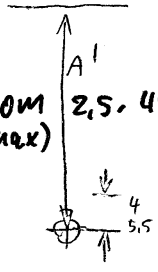
F Anschlag zu 1. Teleskopbef.

A Oberkante zu Teleskopmitte

1HE=44,45			H	h	D	F	A	A+D=	A'
6HE 266,7	P800	BMB 4	265	262	1	53	50		51
1HE		BMB 5		~~265~~			~~50~~		
3HE 133,35		E2 linke Seite!	132	130	1	94	113		114
4HE 177,8	P833		177	171	1	94	113		114
6HE 266,7	P830		266	253 249	8 12	94	194 190	Frontplatte Seitenwand	202

P800

		breite Schiene oben −13	breite Schiene unten +4	schmale Schiene +5,5	A'	oberer Spalt bei br	oberer Spalt bei sch.
BMB 	nom (max) 1,5 · 44,45 = 66,675	53,675	70,675	72,175	51	2,7	
E2 	nom (max) 2,5 · 44,45 = 111,125	98,125	115,125	116,625	114	1,1	2,6
TK 	nom (max) 2,5 · 44,45 = 111,125						
FD 	nom (max) 4,5 · 44,45 = 200,025	187,025	204,025	205,525	202	2	3



TMA increment 1 (020, 021, 022, ...)
PCA " 50 (300, 350, 400, ...)

Manual AA (13, 12, 79)

Models

TMA 757 44 001 ... 020 = BR803 A ... (except U)
021 ... 062 BR8A
except 040 = BR8A2M

PCA 758 90 300 ... 750
758 96 300
758 92 150
776 14 500

Manual L (31, 5, 78)

TMA 757 44 001 ... 61 except 040 as above

PCA 758 90 300 .. 750

ECO

PCA 778 37 850 .. 950
778 38 800, 820, 850, 880
778 39 110, 130, 150

Manual A (77)

TMA 757 44 001 ... 059 including 040 = BR8A2 M

100V 240V 100V
040 ≙ L, M, N

CDC-Floppy

	DOWN = ACTIVE	DOWN = OFF	
7		0	N.C.
6		0	N.C.
5	0		* TERM. (Door unlock 4)
4	0		INT. ERASE ENB
3		0	EXT ERASE ENB
2		0	EXT. ERASE ENB ACT L/H
1	0		* TERM. (Erase enb)

	DOWN = ACTIVE	DOWN = OFF		
8		0	4	RDY
7		0	3	RDY
6		0	2	RDY
5	0		1	RDY
4		0	4	SEL
3		0	3	SEL
2		0	2	SEL
1	0		1	SEL

* these plus network RM2 in last drive of daisy chain only

CDC Floppy

					9406		9404	
	50				TYPE	○	UNL	S3
(S12)	48	47	COM	nc	UNL2		□	RM
(S11)	46	45	COM	nc	WRFR		□	
(EQA)	44	43		nc	WRF		□	
	42				UNL1		□	RM
	40				SIDE	○	UNL	RM
	38				ERA			
	36				WP		□	
	34				RY4		□	
	32				RY3		□	
	30				RY2		□	
	28				RY1		□	
	26				SEL4		□	
	24				SEL3		□	
	22				SEL2		□	
	20				SEL1		□	
	18				WDA		□	
	16				WRE		□	
	14				DIR		□	
	12				STEP		□	
	10				LWC		□	
	8				IND		□	
	6				TRK0		□	
	4				HLD		△	
	2				RDA		□	

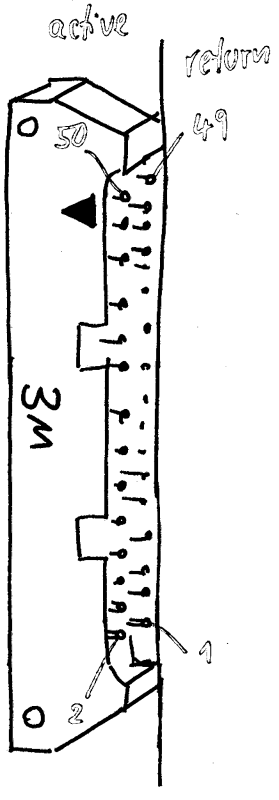
Conclusions:

1) Mixed configuration for drives without download only!

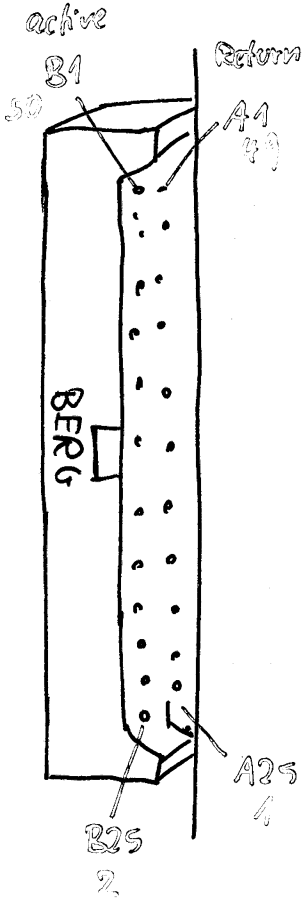
2) Pin 50: Output on 9406 (open = H = single sided) (active L = double sided)
Input on 9404, terminated via S3-5 which must be open anyway

3) Controller must be switched to 9406

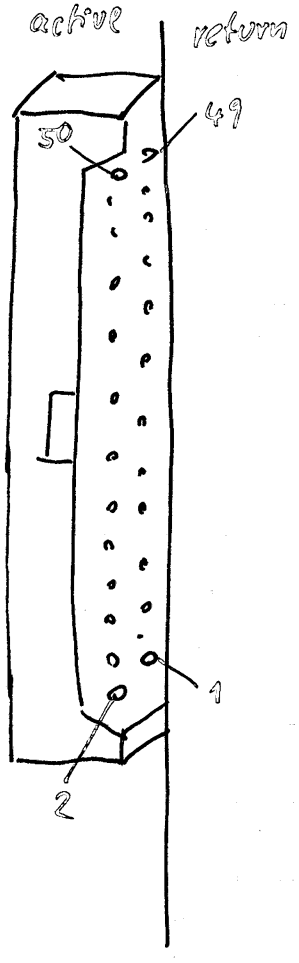
CDC



FIMZA



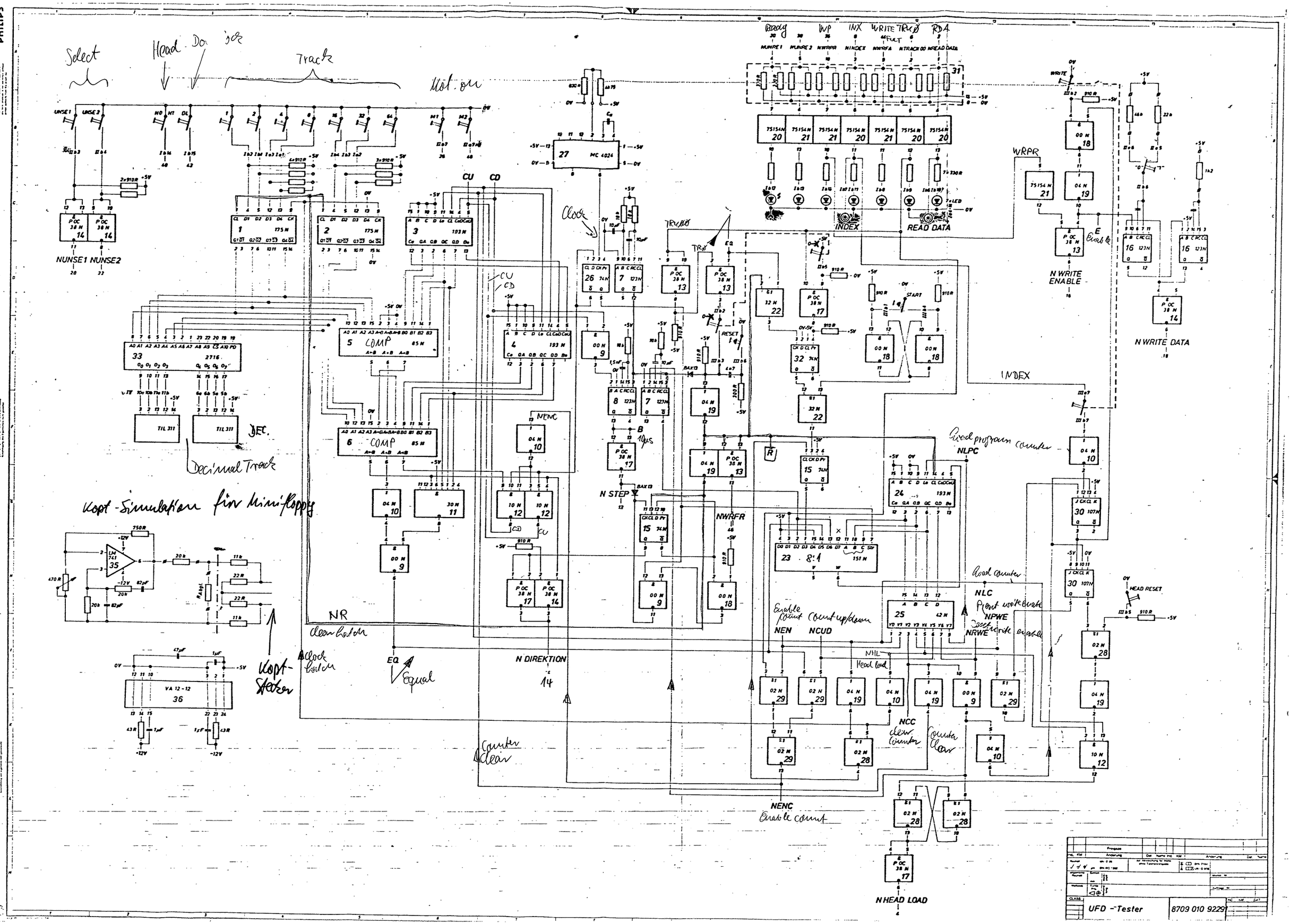
FLDZ



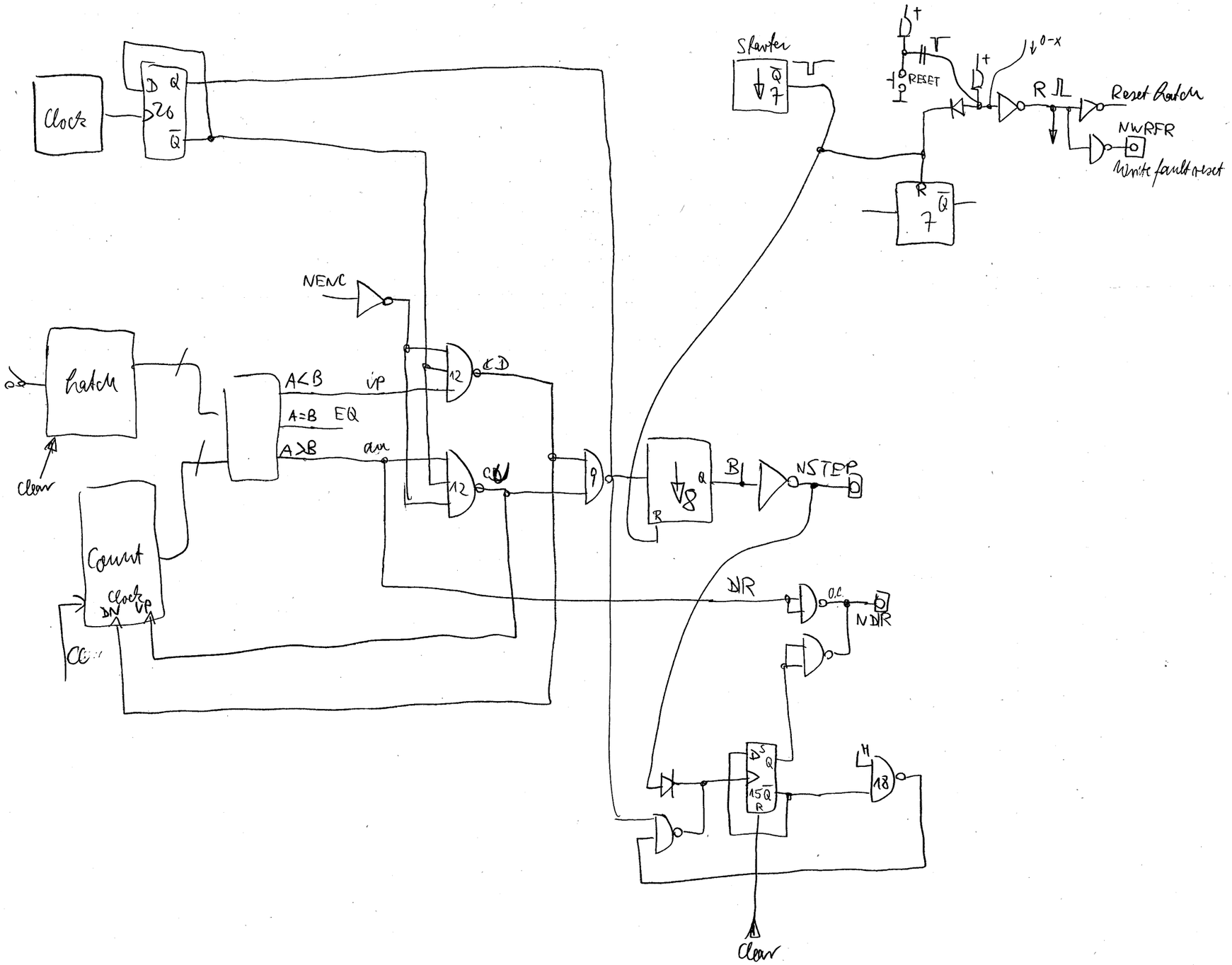
Inscription on PCB

" " in manual

P830



Select
Head
Track
Mot. on
NUNSE1 NUNSE2
Decimal Track
DEC.
Kopt-Simulation für Minifloppy
Kopt-Stecker
Clock
Ready
WP
INX
WRITE TRK0
RDA
INDEX
READ DATA
WRPR
N WRITE ENABLE
N WRITE DATA
INDEX
Load program counter
NLPC
N STEP
NWRFR
NR
clear latch
Clock latch
EQ
Equal
N DIREKTION
NEN
NCUD
NLC
NPWE
NRWE
NHL
Head load
NCC
clear counter
Counter clear
NENC
Enable count
N HEAD LOAD
HEAD RESET
UFD - Tester
8709 010 9229

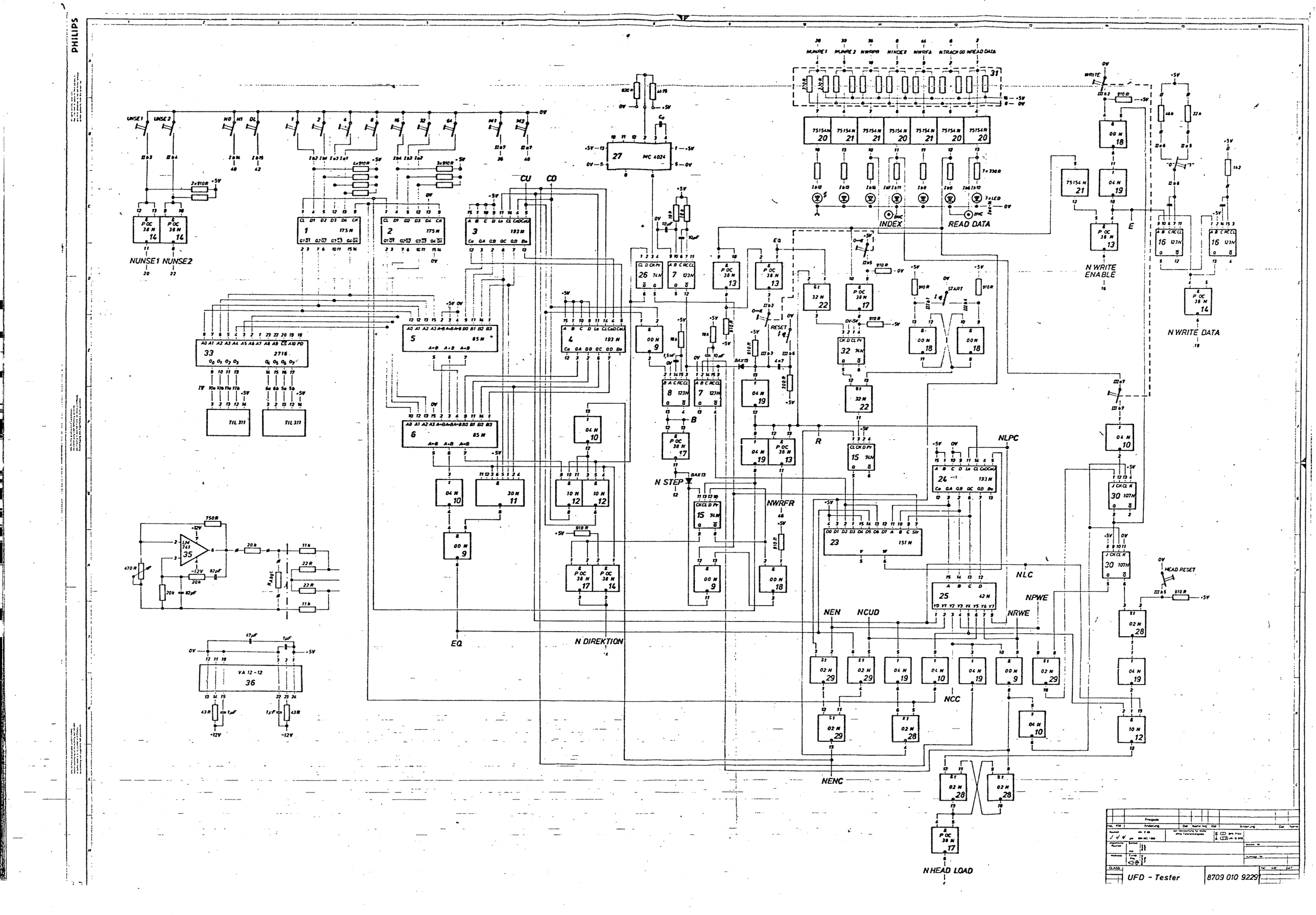


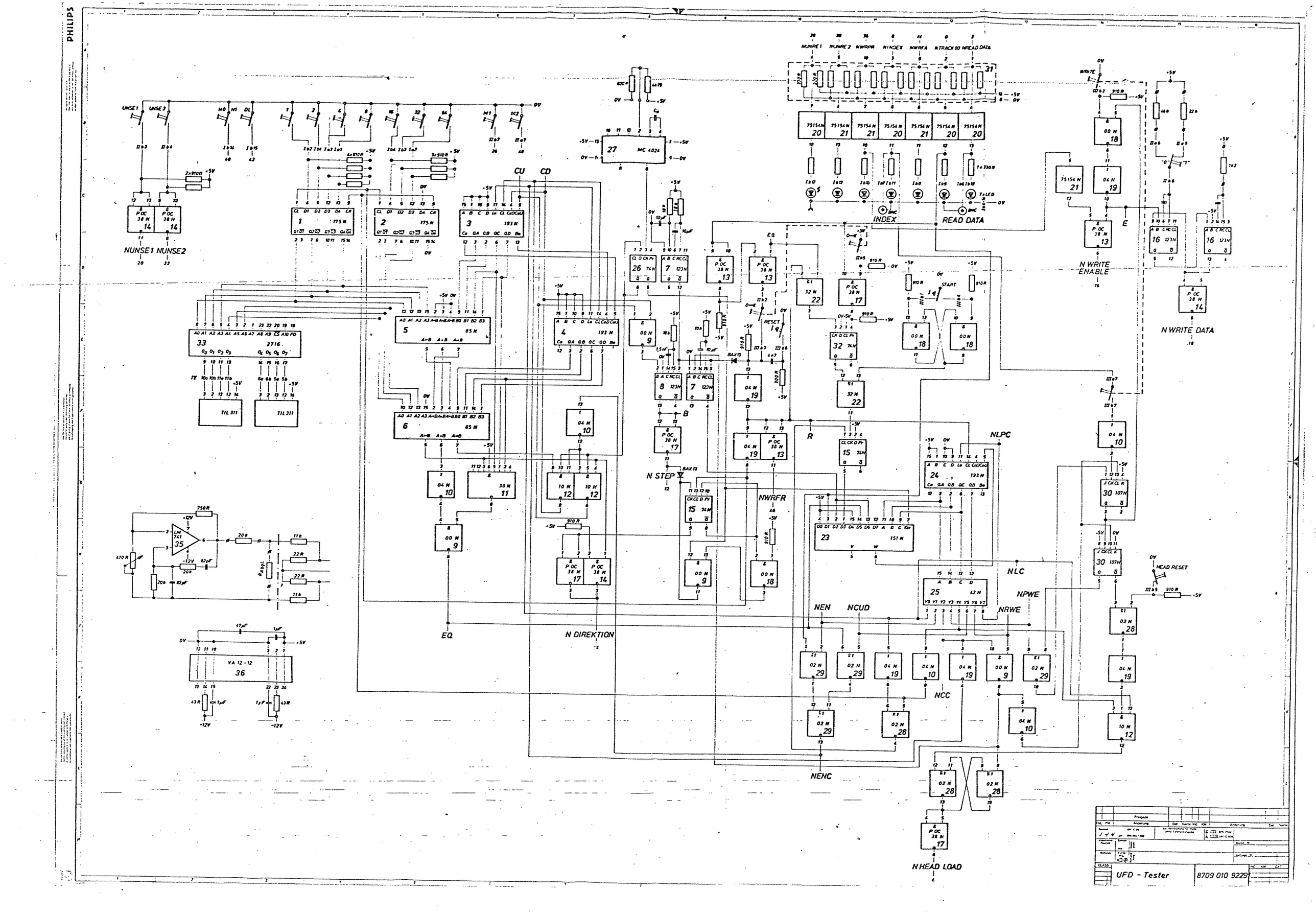
Floppy-Tester

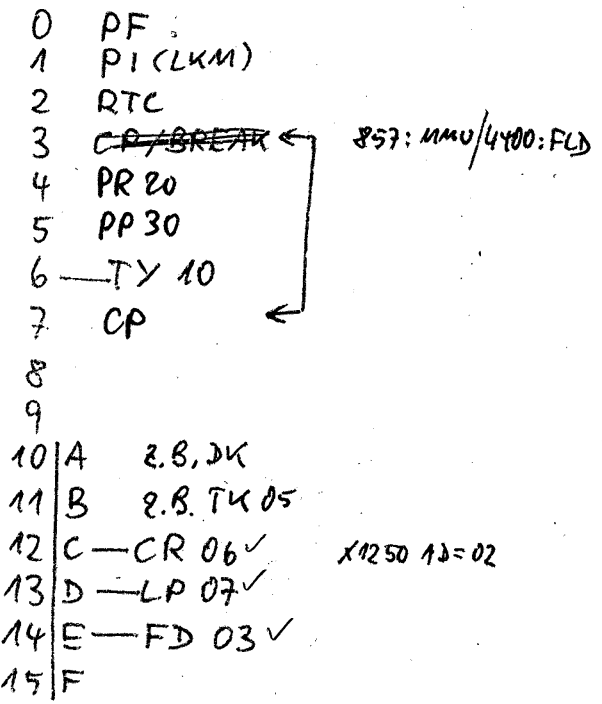
PHILIPS

UFD - Tester

8709 010 9229


PHILIPS
NUNSE1 NUNSE2
CU
CD
INDEX
READ DATA
N WRITE ENABLE
N WRITE DATA
START
RESET
N STEP
NWRFR
NLPC
NLC
NPWE
NRWE
NEN
NCUD
NCC
NENC
N DIREKTION
EQ
HEAD RESET
N HEAD LOAD
TIL 311
VA 12-12
UFD - Tester
8709 010 9229


PHILIPS
NUNSE1 NUNSE2
CU
CD
INDEX
READ DATA
N WRITE ENABLE
N WRITE DATA
N STEP
NWRFR
NLPC
NLC
NPWE
NRWE
NEN
NCUD
NCC
NENC
EQ
N DIREKTION
N HEAD LOAD
HEAD RESET
TIL 311
VA 12-12
UFD - Tester
8709 010 9229


0 PF
1 PI (LKM)
2 RTC
3 ~~CP/BREAK~~
4 PR 20
5 PP 30
6 TY 10
7 CP
8
9
10 A z.B. DK
11 B z.B. TK 05
12 C CR 06 ✓
13 D LP 07 ✓
14 E FD 03 ✓
15 F
857: MMU/4400: FLD
X1250 10=02

4400/851

0		(PWF)
1		LKM
2		RTC
3		FLD
4		IEC/PR
5		IEC/PP
6		KB
7		CP
8		
9		DC
10	A	DC
11	B	DC
12	C	DC
13	D	(LP)
14	E	
15	F	SCUZ

17E = $\overset{B}{\sim}$

Euro-controller tests

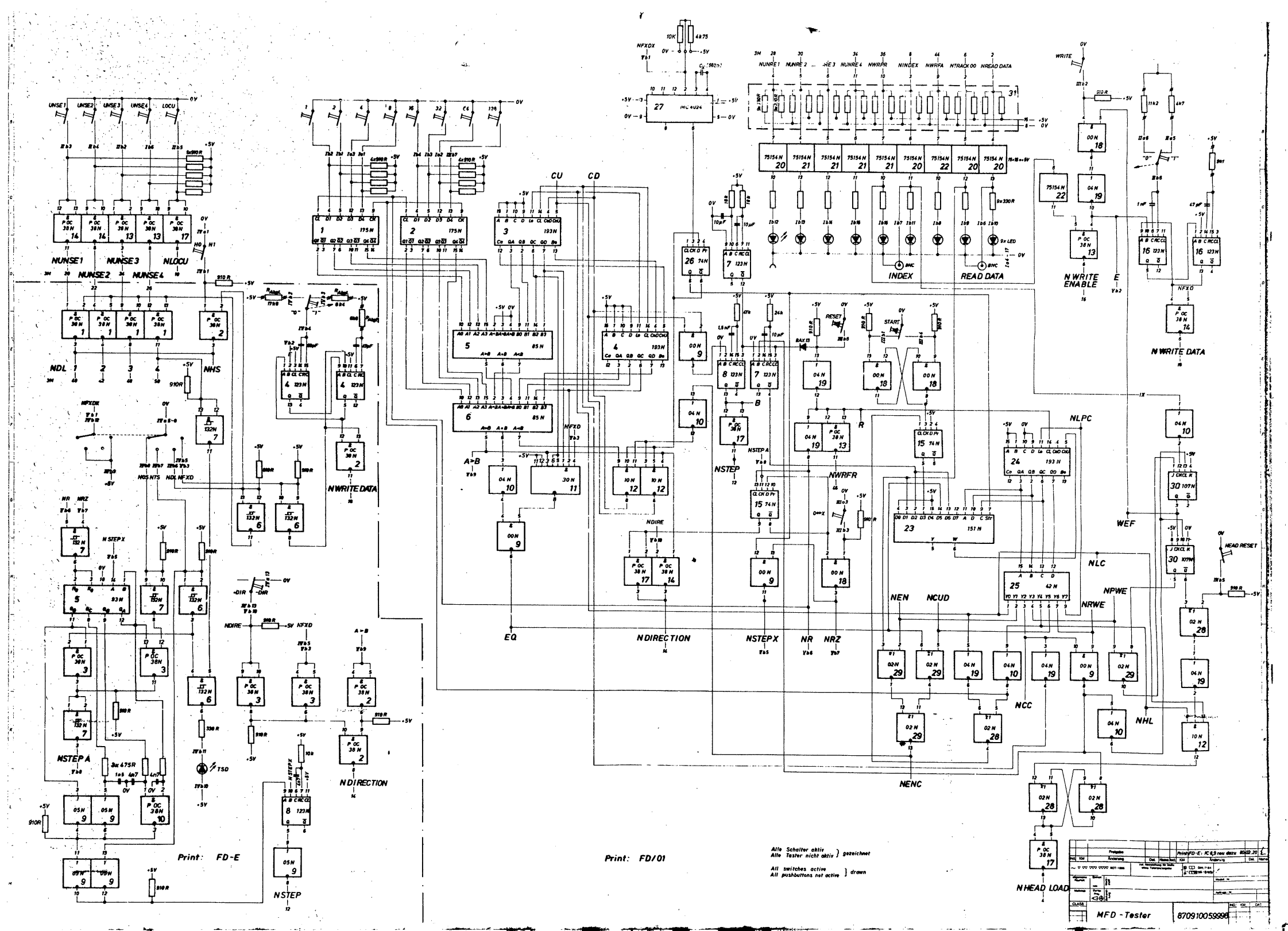
X1250 AD=/02 IR=12=/0C

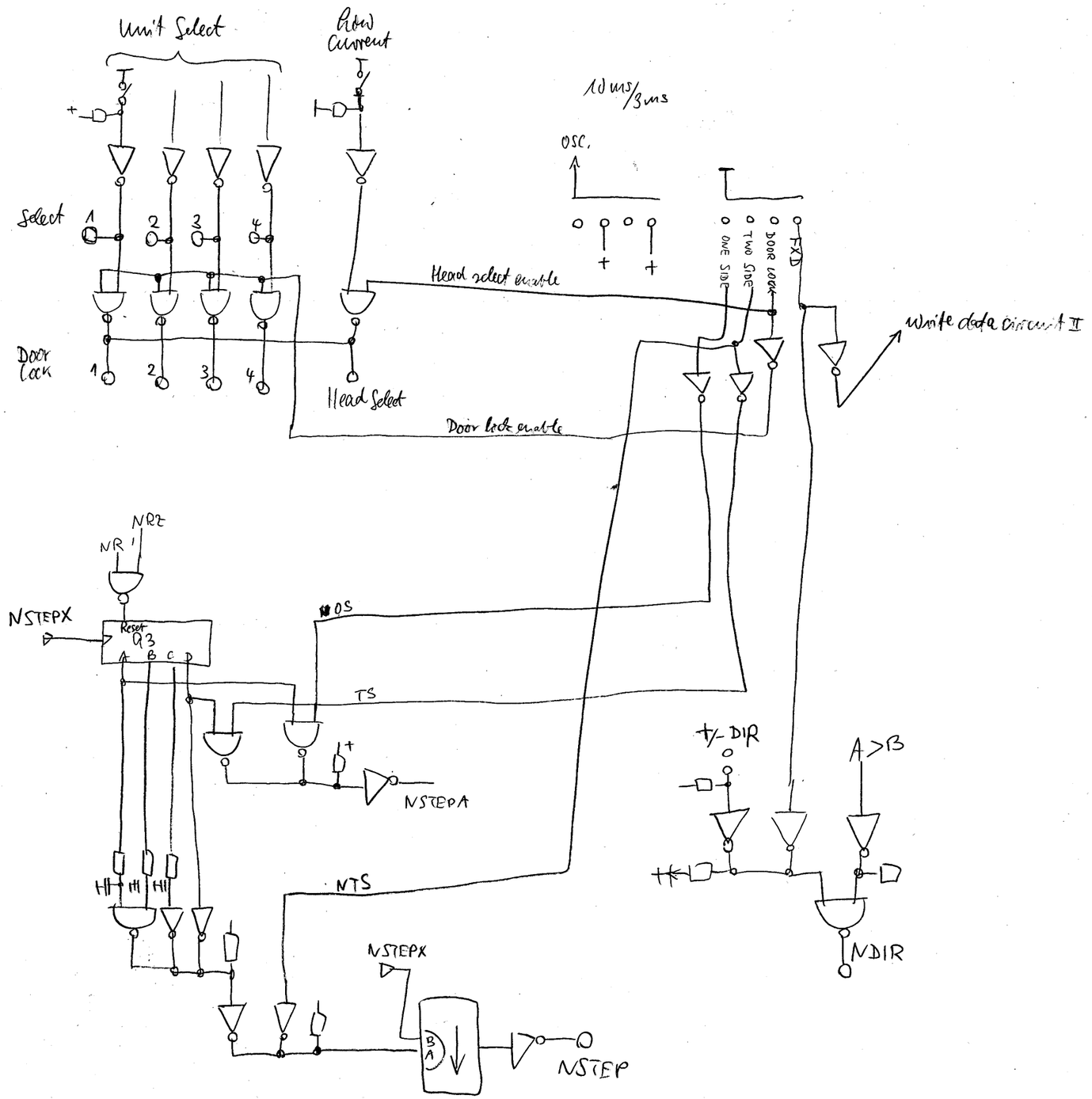
X1216 } AD=/02 IR=/ =10
X1215 }

FD1M ?

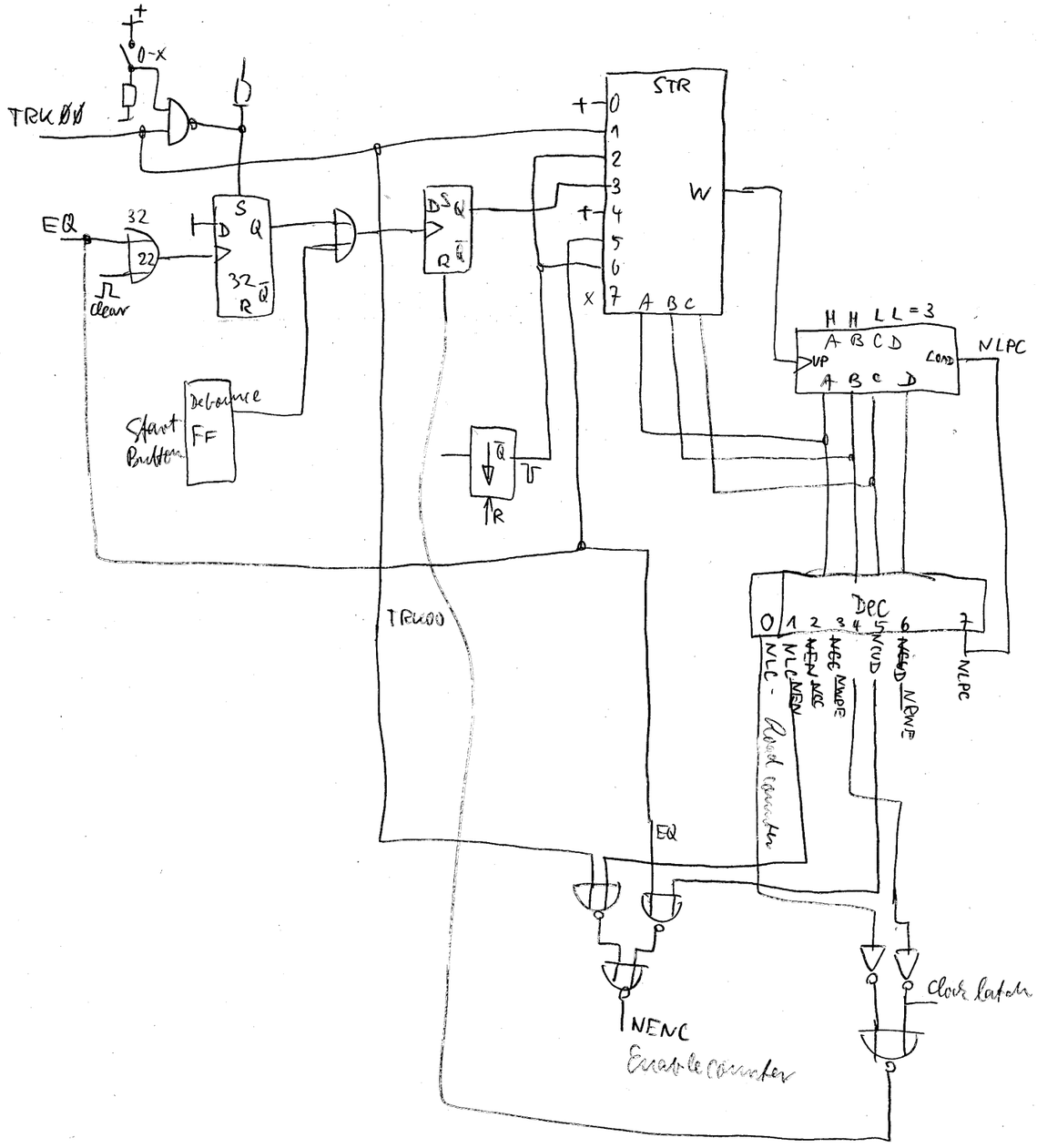
FD2504 AD=/03 IR=/E

SCUZ AD=/10 IR=/6


Print: FD-E
Print: FD/01
Alle Schalter aktiv
Alle Taster nicht aktiv } gezeichnet
All switches active
All pushbuttons not active } drawn
MFD - Tester
8709100599901

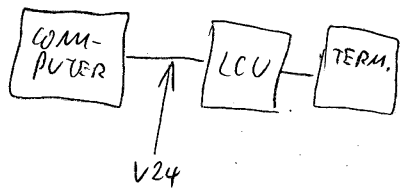

Unit Select
Row Current
10 ms/3 ms
OSC.
Select
1
2
3
4
Door Lock
Head select enable
Head Select
Door lock enable
ONE SIDE
TWO SIDE
DOOR LOCK
FXD
Write data circuit II
NRZ
NRZ'
NSTEPX
Reset
Q3
A B C D
OS
TS
NSTEPA
NTS
NSTEPX
B
A
NSTEP
+/- DIR
A>B
NDIR

MFD-Tester



TRK00
0-X
EQ
32
22
clear
S
D
Q
32
R
Q̄
Start Button
Debounce
FF
STR
W
A B C
H H L L = 3
A B C D
UP
LOAD
NLPC
DEC
NLC
NLC
NEN
NCC
NWPE
NCUD
NRWE
NLPC
Road counter
TRK00
EQ
NENC
Enable counter
Clock latch

MFD-Tester



4.4 CCITT INTERFACE TABLE

Interface circuits in accordance with CCITT-V24

LCU (Line control unit) ≙ data terminal unit

Circuit	PIN	Signal	Description	Direction
101	1	Pin 01	Protective ground/earth	
102	7	Pin 07	Signal ground/common return	
103	2	TMD	Transmitted data. The data which is transmitted, modulated by modem or not modulated.	From LCU
104	3	RCD	Received data. The data which is received, de-modulated by modem, or not modulated at all.	To LCU
105	4	RTS	Request to send. This signal functions in co-operation with a connected modem and means switch on the transmitter. In a configuration without modems, the signal RTS is connected to RFS.	From LCU
106	5	RFS	Ready for sending. If this signal is ON, it indicates that the modem has switched-on its transmitter upon RTS. Delay between RTS and RFS is called τ 106.	To LCU
107	6	DSR	Data set ready. If ON, this signal indicates that the modem is ready to operate.	To LCU
108.1	20	CDSL	Connect data set to line. If ON, this signal switches the modem on the line, if OFF, the modem is switched-off the line.	From LCU
108.2		DTR	Data terminal ready. The ON condition indicates that the modem is ready to operate and is connected to the line. The OFF condition indicates that the modem is switched-off the line and is not ready to operate.	From LCU
109	8	DCD	Data carrier detected. If ON, this signal indicates that the modem has detected a signal (carrier) on the line which is within the appropriate limits.	To LCU
111	23	DSRS	Data signalling rate selector. Signal to select one out of two possible data signalling rates (transfer rates) or ranges of rates.	From LCU
113		TSET(M)	Transmitter signal element timing. Synchronous clockpulse for the transmitting circuits in the LCU (timing in LCU).	From LCU
114	15	TSET	Transmitter signal element timing. Synchronous clockpulse for the transmitting circuits in the LCU (timing in modem).	To LCU
115	17	RSET	Receiver signal element timing. Synchronous clockpulse for the receiving circuits in the LCU.	To LCU
125	22	CIN	Calling indicator. This signal is only applicable in modems at LCU-side. It becomes ON as soon as the remote terminal operator has made a call to become connected to the LCU in switched networks.	To LCU
126		STF	Select transmit frequency. This signal is used, to select the required transmit frequency.	From LCU

Pin 1 used:
9
11
19
25

Figure 1-19 INTERFACE TO DATA CIRCUIT EQUIPMENT

There are still some interface lines which are not used by the DCE. These lines may serve as auxiliary interface to the linetest equipment, they are:

RRCD' Regenerated Received data
RRSET' Regenerated Receiver Signal Element Timing
RTSET' Regenerated Transmitter Signal Element Timing
RTMD' Transmitted data from test equipment (Transceiver).

When there is used a built-in inplant modem the above mentioned interface becomes internal interface. To the line side however, now 4 pins have to be reserved, they are:

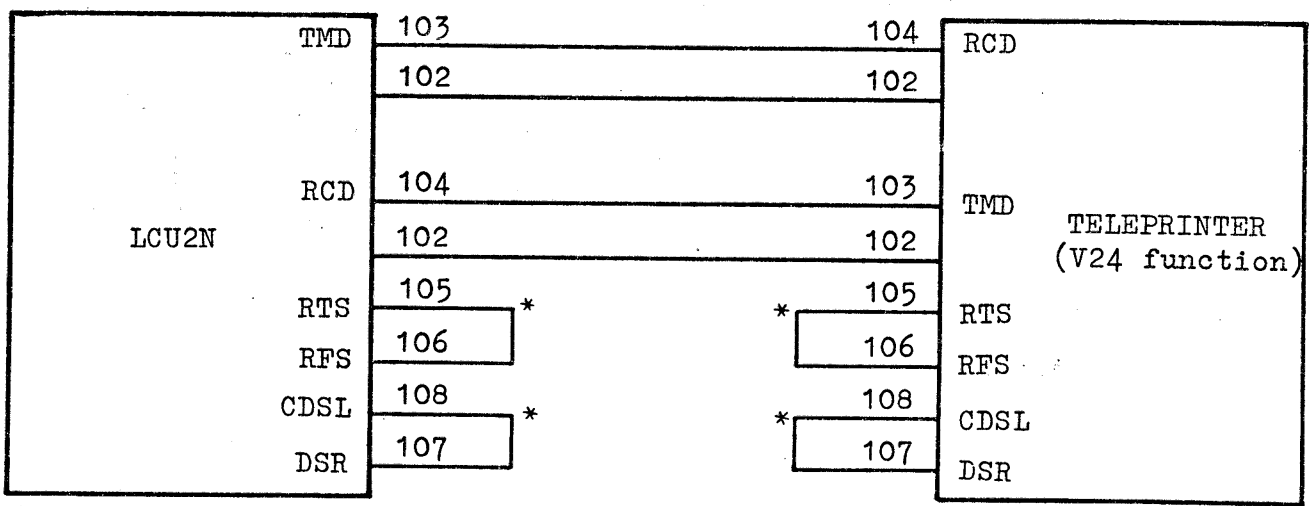
DOUT0 - Data out 0
DOUT1 - Data out 1
DIN0 - Data in 0
DIN1 - Data in 1

for pin occupation see figure 1-22 and 1-23

4.5 CCITT LINE VALUE REFERENCE

CCITT V24	≤ -3V	≥ +3V
Binary value	1	0
Data circuit	mark	space
Timing/Control circuit	OFF	ON

4.6 OPERATION WITHOUT DATA CIRCUIT EQUIPMENT



*Interconnections in plug. Plugs at LCU2N and terminal are interchangeable.

Figure 1-20 OPERATION WITHOUT DCE

For short distance inplant connections (< 1000 m), the relevant interchange circuits on control unit and teleprinter side are connectable directly without DCE in between. This is only applicable to the LCU-2N. The electrical characteristics of the interchange circuits shall allow a transmission performance comparable to that for a link with DCE.

4.7 OPERATION ON LEASED TELEPHONE LINE (LCU-2N AND LCU5)

The interface between LCU-2N and the modem (CCITT-V21) is in accordance with the CCITT-V24 recommendation.
Only the receiving and transmitting data circuits are applied. Controlling and signalling circuits which are available on the modem are not all used, because there is a permanent connection.

4.8 OPERATION ON PUBLIC SWITCHED NETWORKS

Although connections to certain data circuit-equipment may not require all interchange circuits listed in figure 1-19, the LCU2NS and LCU5 shall be capable to handle the mentioned circuit if necessary for the connected equipment.
There will be some deviations in use of interchange circuits. Connection to a line in a switched network is established automatically on a call from a remote station. The following modes of operation will be possible:

1. Use of functions 108/1 and 105
2. Use of functions 108/1 no "request to send" facility
3. Use of functions 108/2 and 105
4. Use of functions 108/2 no "request to send" facility

The mode 1 shall be Standard implemented. Changing to the other modes is possible, eventually by straps in the control unit.

The sequence of signals for switching on and off in mode 1 is shown below, without relation to time.

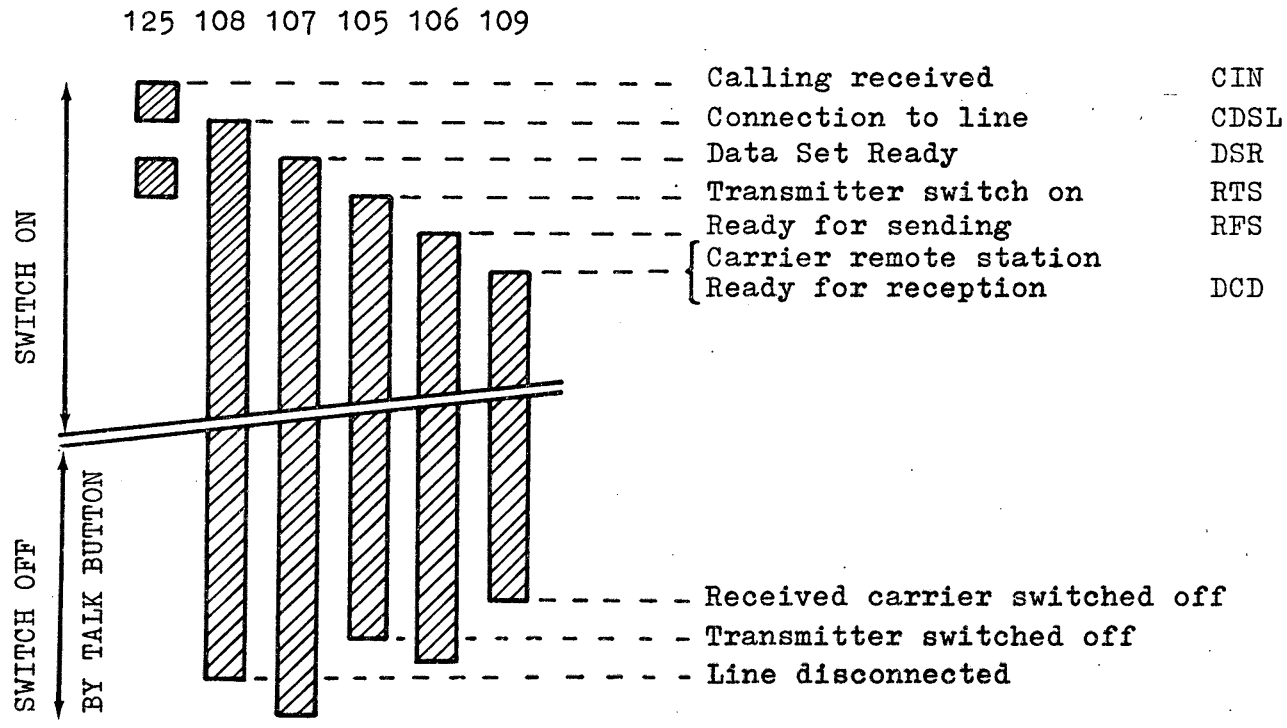


Figure 1-21 SWITCHING ON AND OFF (108/1)

More information will be given in Connecting Procedure - Volume 3 - chapter 11.

4.9 CCITT INTERFACE PLUG OCCUPATION

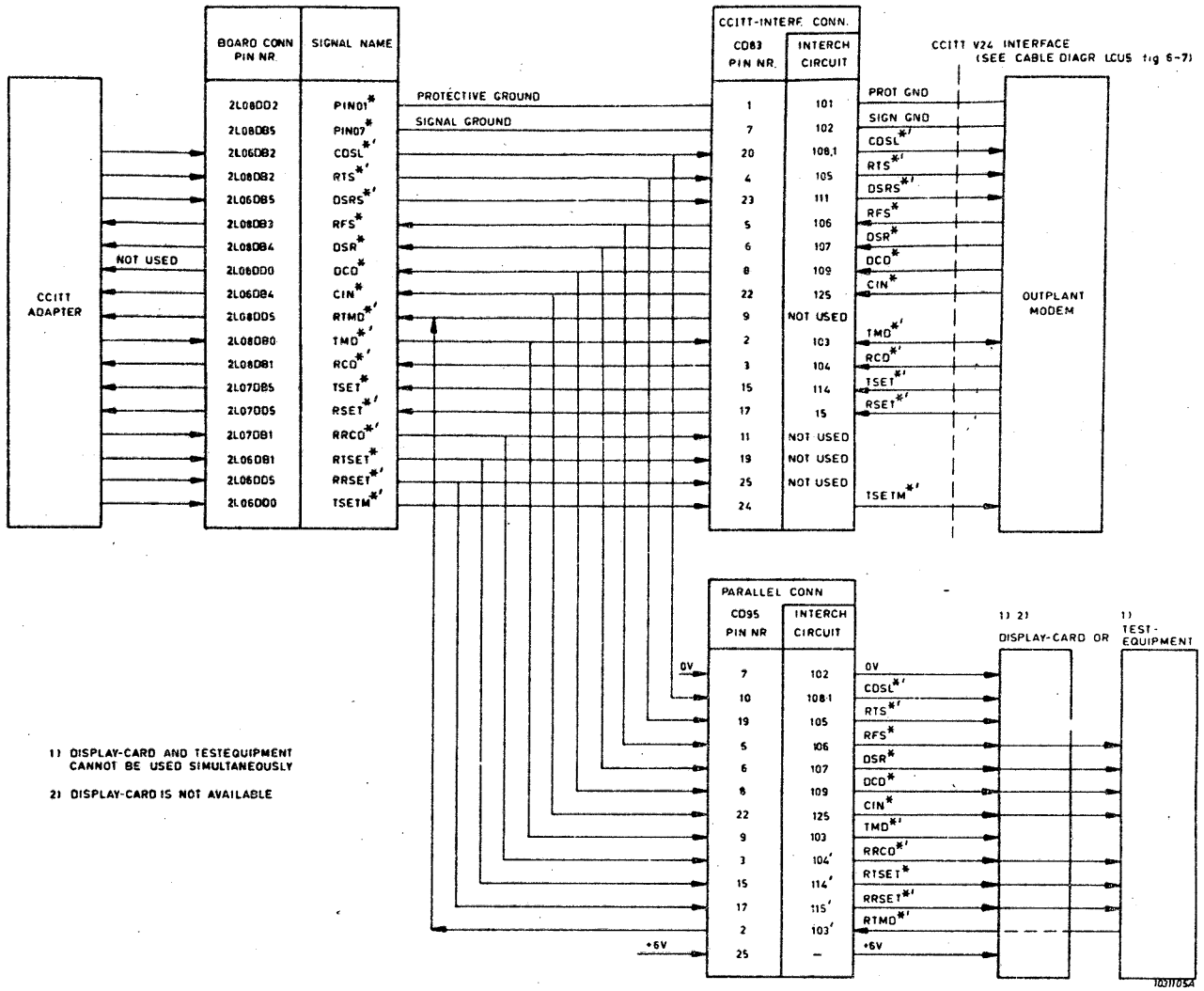


Figure 1-22 INTERFACE TO OUTPLANT CONFIGURATION

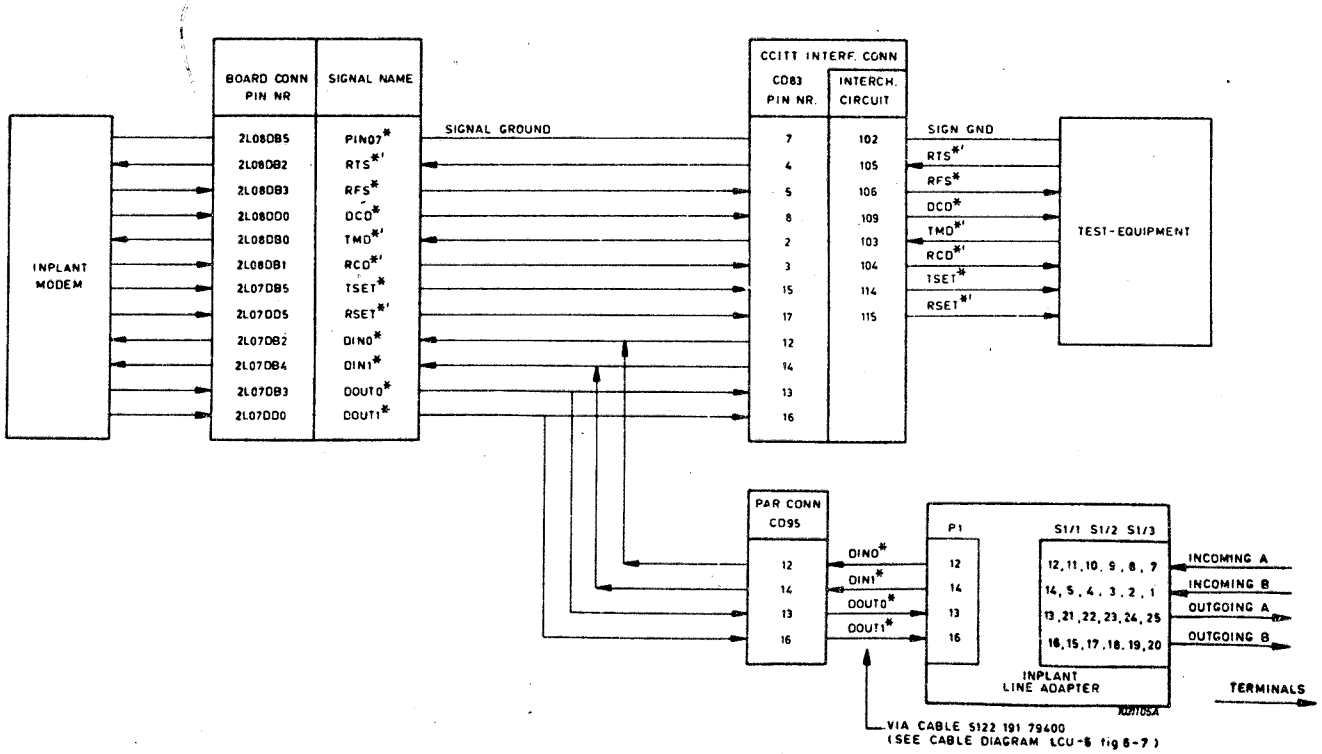
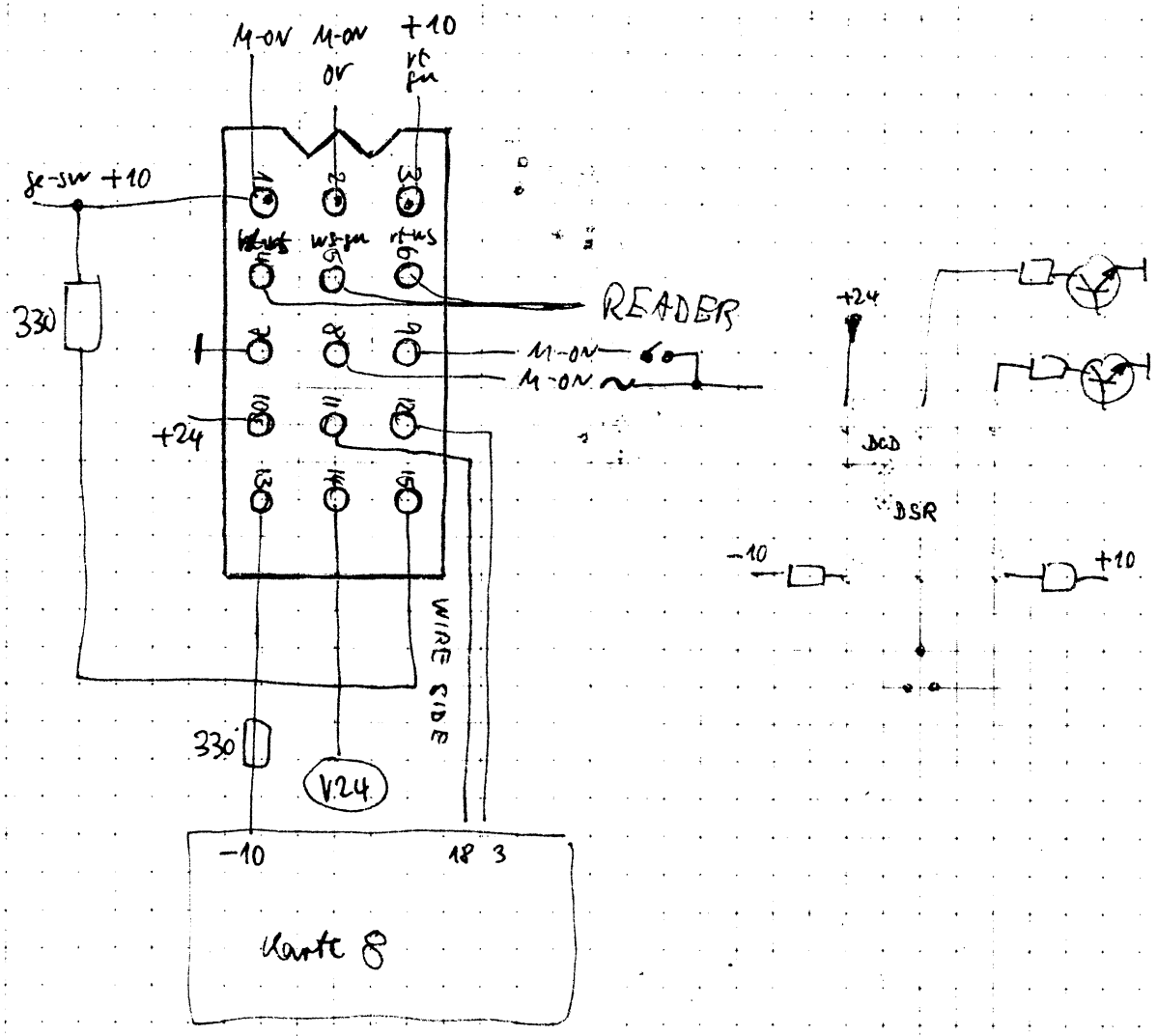


Figure 1-23 INTERFACE TO INPLANT CONFIGURATION

Interface



M-ON
M-ON
0V
+10
rt
gn
ge-sw +10
330
READER
M-ON
M-ON
+24
WIRE SIDE
330
V24
-10
18 3
Karte 8
+24
DCD
DSR
-10
+10

4.4 CCITT INTERFACE TABLE

Interface circuits in accordance with CCITT-V24

Circuit	Signal	Description	Direction
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106	RFS	Ready for sending. If this signal is ON, it indicates that the modem has switched-on its transmitter upon RTS. Delay between RTS and RFS is called τ 106.	To LCU
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108.1	CDSL	Connect data set to line. If ON, this signal switches the modem on the line, if OFF, the modem is switched-off the line.	From LCU
108.2	DTR	Data terminal ready. The ON condition indicates that the modem is ready to operate and is connected to the line. The OFF condition indicates that the modem is switched-off the line and is not ready to operate.	From LCU
109	DCD	Data carrier detected. If ON, this signal indicates that the modem has detected a signal (carrier) on the line which is within the appropriate limits.	To LCU
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125	CIN	Calling indicator. This signal is only applicable in modems at LCU-side. It becomes ON as soon as the remote terminal operator has made a call to become connected to the LCU in switched networks.	To LCU
126	STF	Select transmit frequency. This signal is used, to select the required transmit frequency.	From LCU

Figure 1-19 INTERFACE TO DATA CIRCUIT EQUIPMENT

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RTSET' Regenerated Transmitter Signal Element Timing
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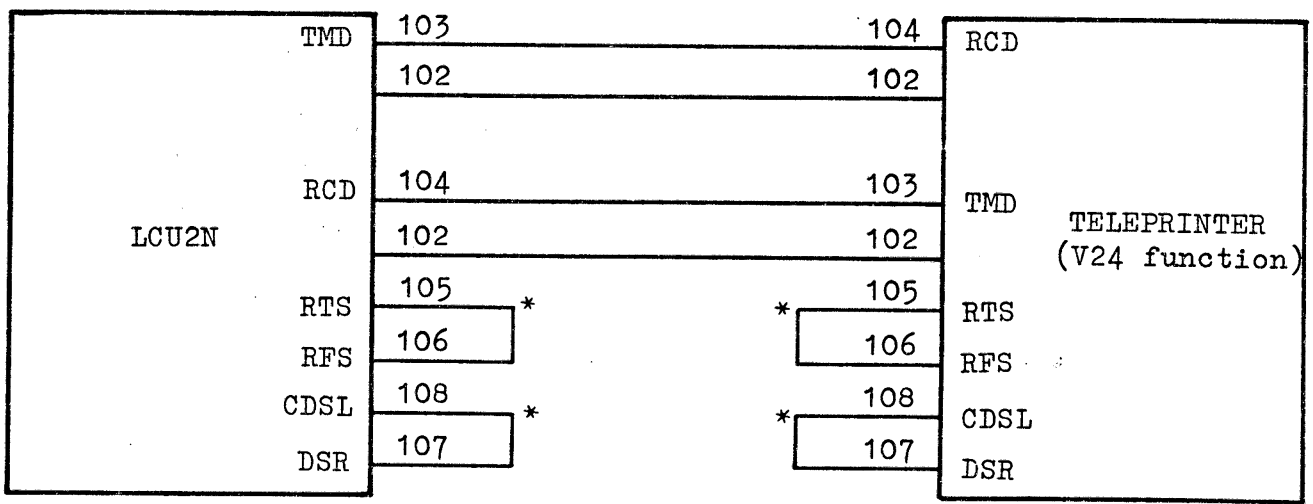
DOUT1 - Data out 1
DIN0 - Data in 0
DIN1 - Data in 1

for pin occupation see figure 1-22 and 1-23

4.5 CCITT LINE VALUE REFERENCE

CCITT V24	≤ -3V	≥ +3V
Binary value	1	0
Data circuit	mark	space
Timing/Control circuit	OFF	ON

4.6 OPERATION WITHOUT DATA CIRCUIT EQUIPMENT



*Interconnections in plug. Plugs at LCU2N and terminal are interchangeable.

Figure 1-20 OPERATION WITHOUT DCE

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2. Use of functions 108/1 no "request to send" facility
3. Use of functions 108/2 and 105
4. Use of functions 108/2 no "request to send" facility

The mode 1 shall be Standard implemented. Changing to the other modes is possible, eventually by straps in the control unit.

The sequence of signals for switching on and off in mode 1 is shown below, without relation to time.

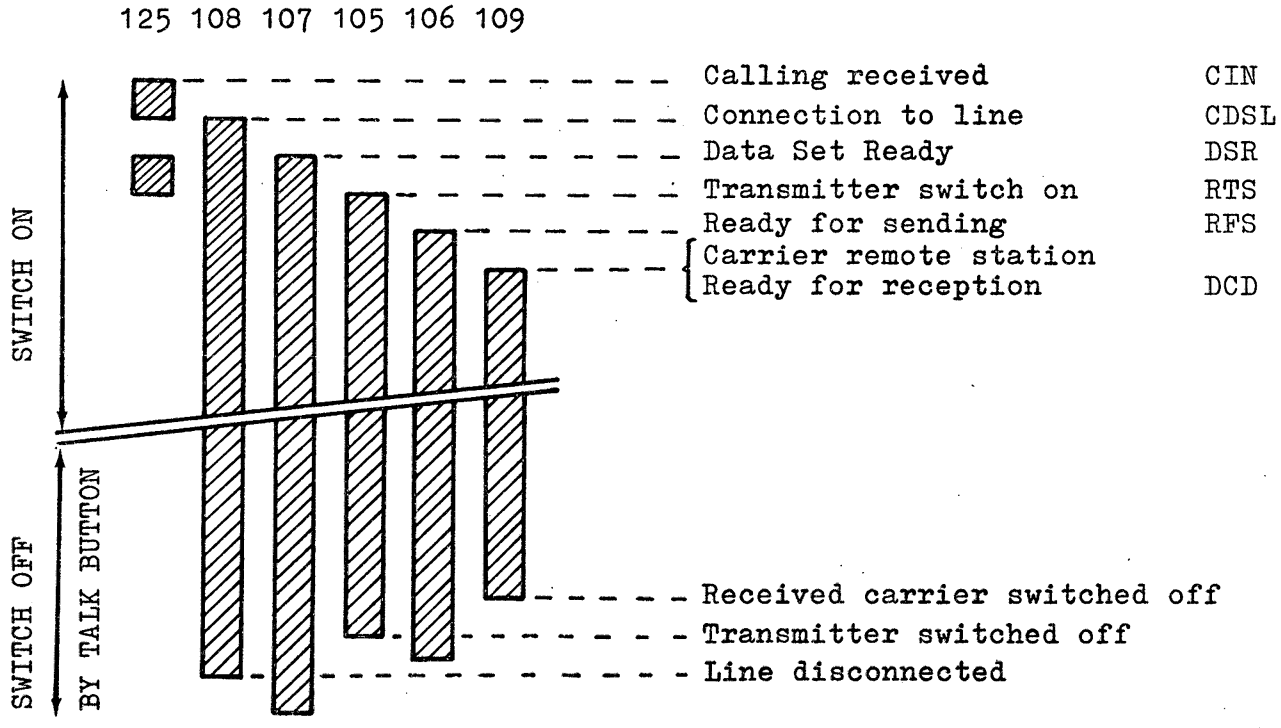


Figure 1-21 SWITCHING ON AND OFF (108/1)

More information will be given in Connecting Procedure - Volume 3 - chapter 11.

4.9 CCITT INTERFACE PLUG OCCUPATION

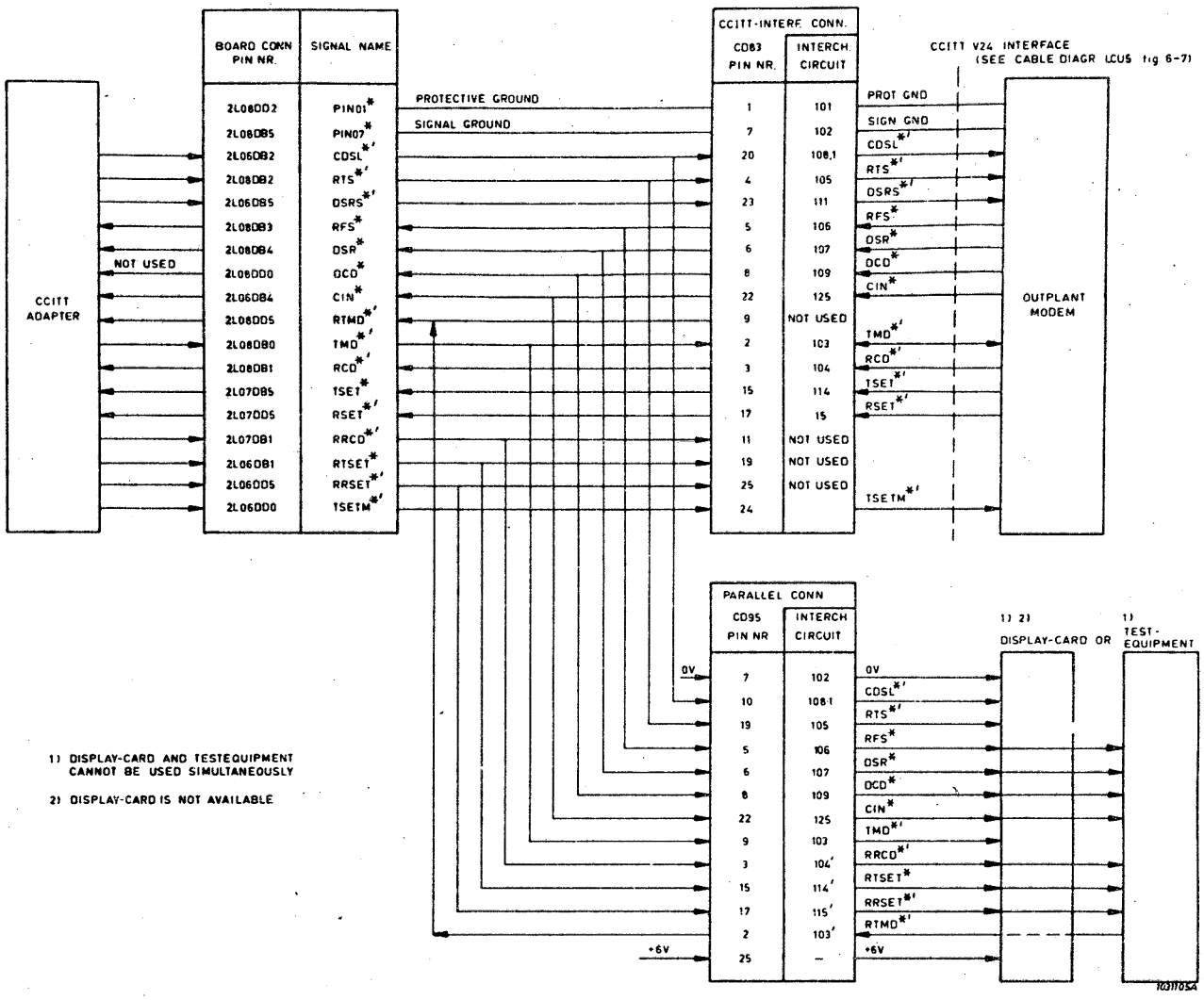


Figure 1-22 INTERFACE TO OUTPLANT CONFIGURATION

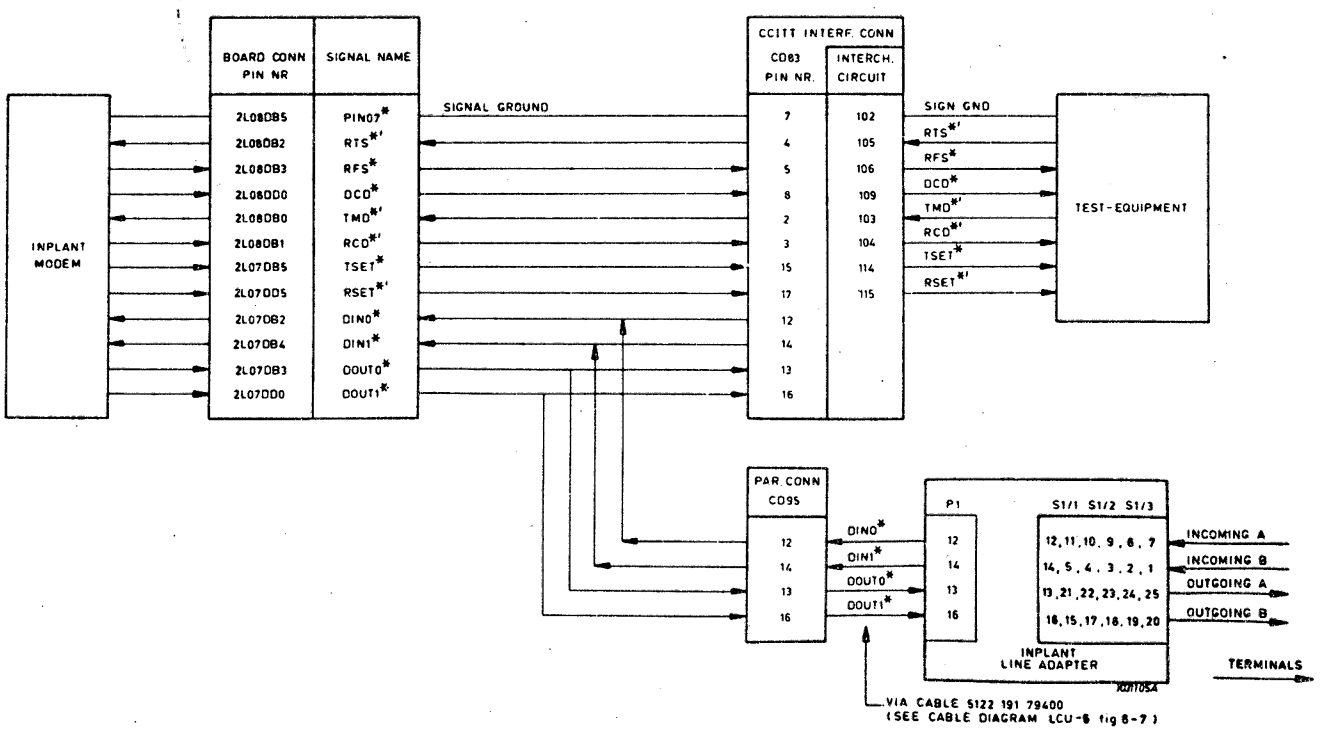
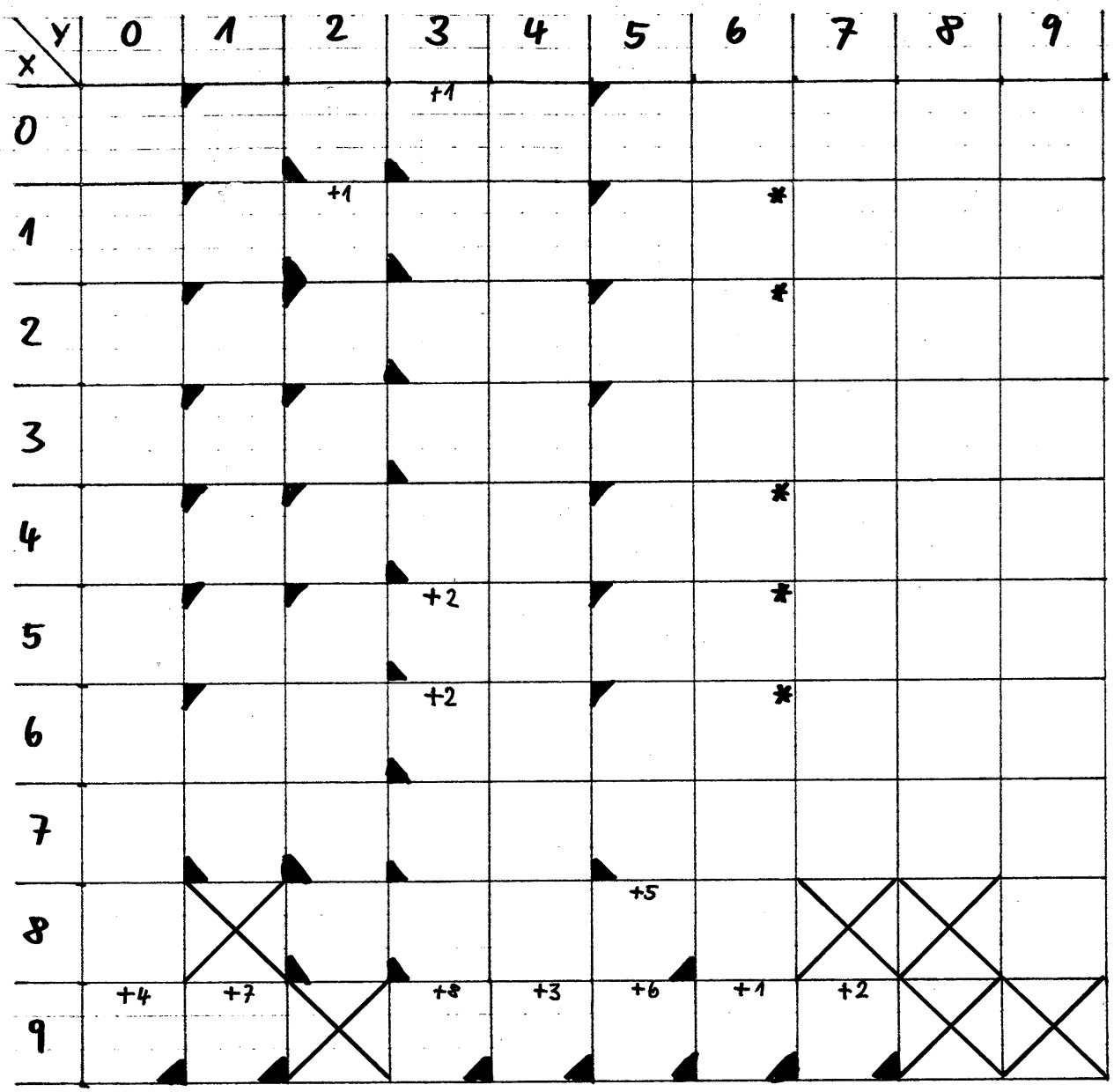


Figure 1-23 INTERFACE TO INPLANT CONFIGURATION



+ INDICATOR POSSIBLE
* VIA NAT.VERS. JMP.

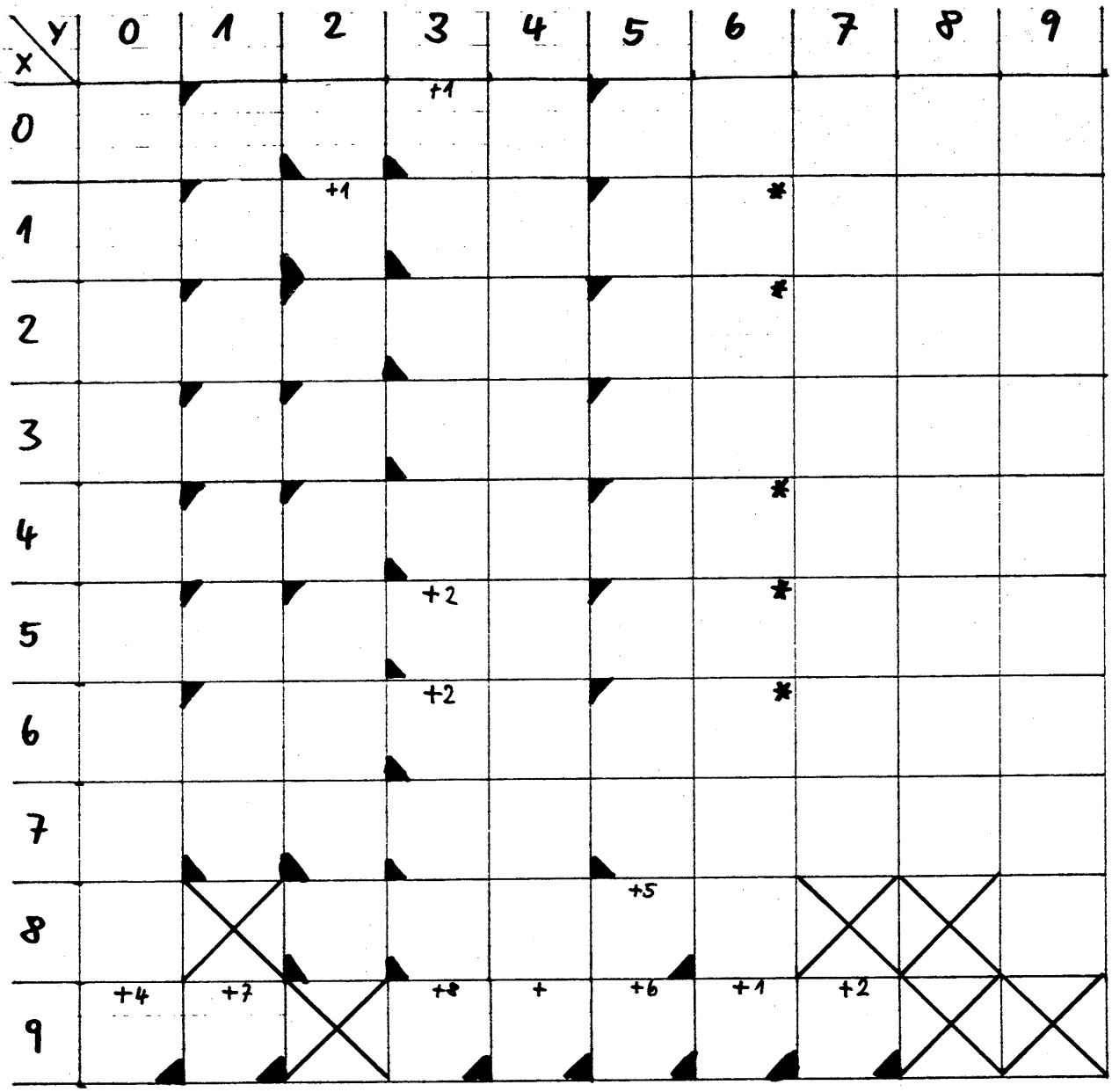
NUM. PAD

CNTR. PAD

ADD. PAD

KEYBOARD MATRIX

MODEL P817



+ INDICATOR POSSIBLE
* VIA NAT.VERS. JMP.

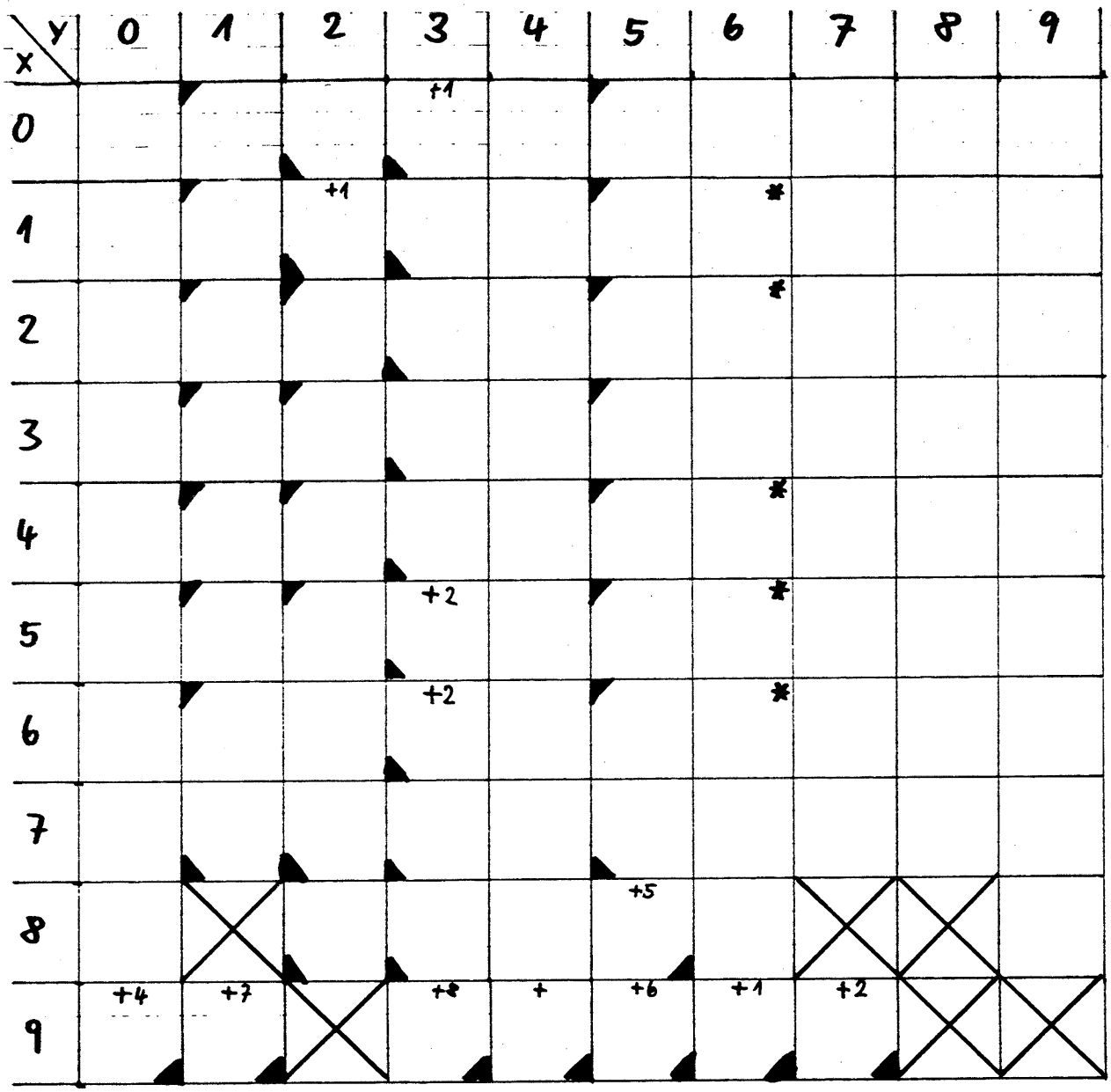
NUM. PAD

CNTR. PAD

ADD. PAD

KEYBOARD MATRIX

MODEL P



+ INDICATOR POSSIBLE
* VIA NAT.VERS. JMP.

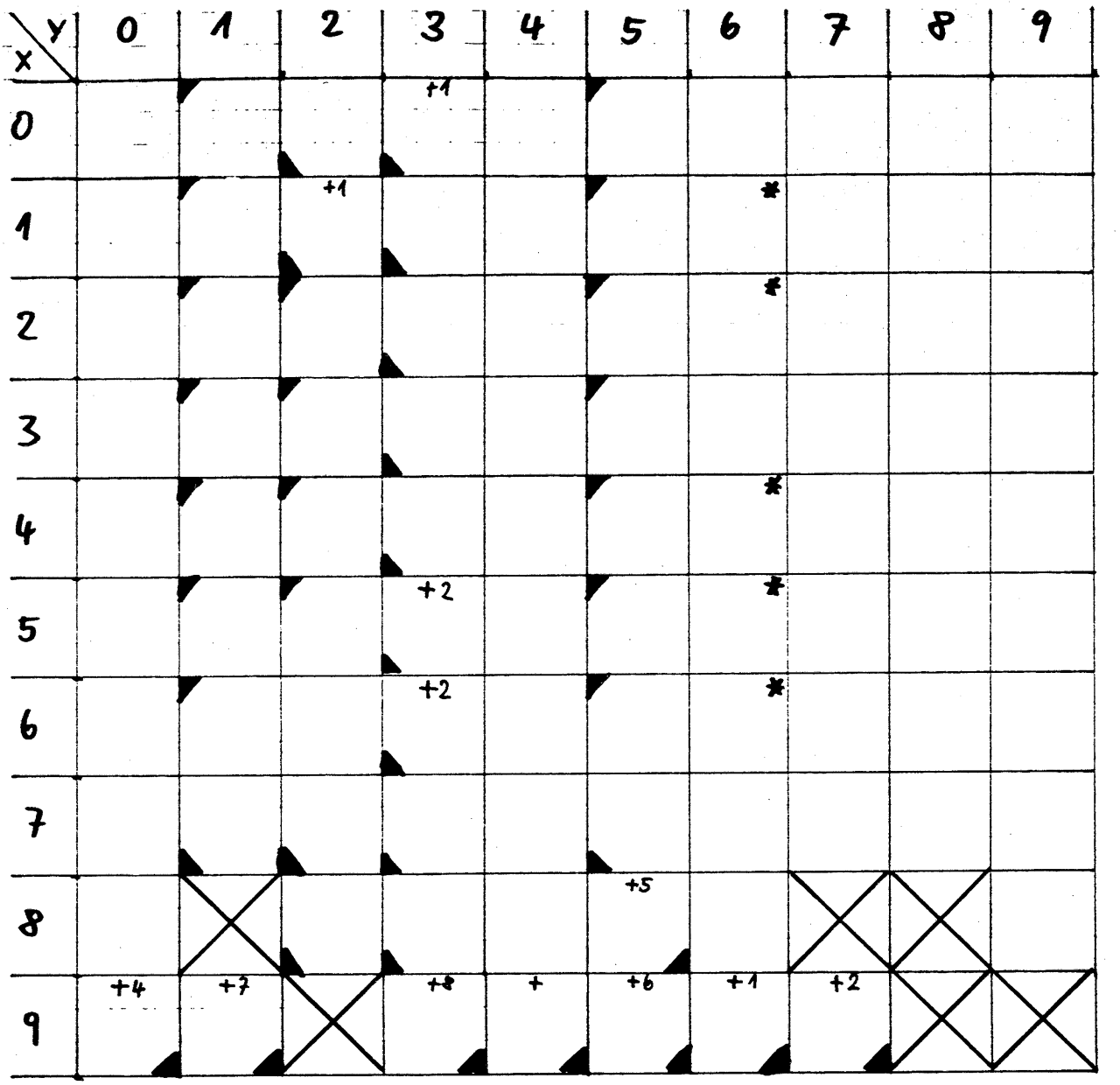
NUM. PAD

CNTR. PAD

ADD. PAD

KEYBOARD MATRIX

MODEL P



+ INDICATOR POSSIBLE
* VIA NAT.VERS. JMP.

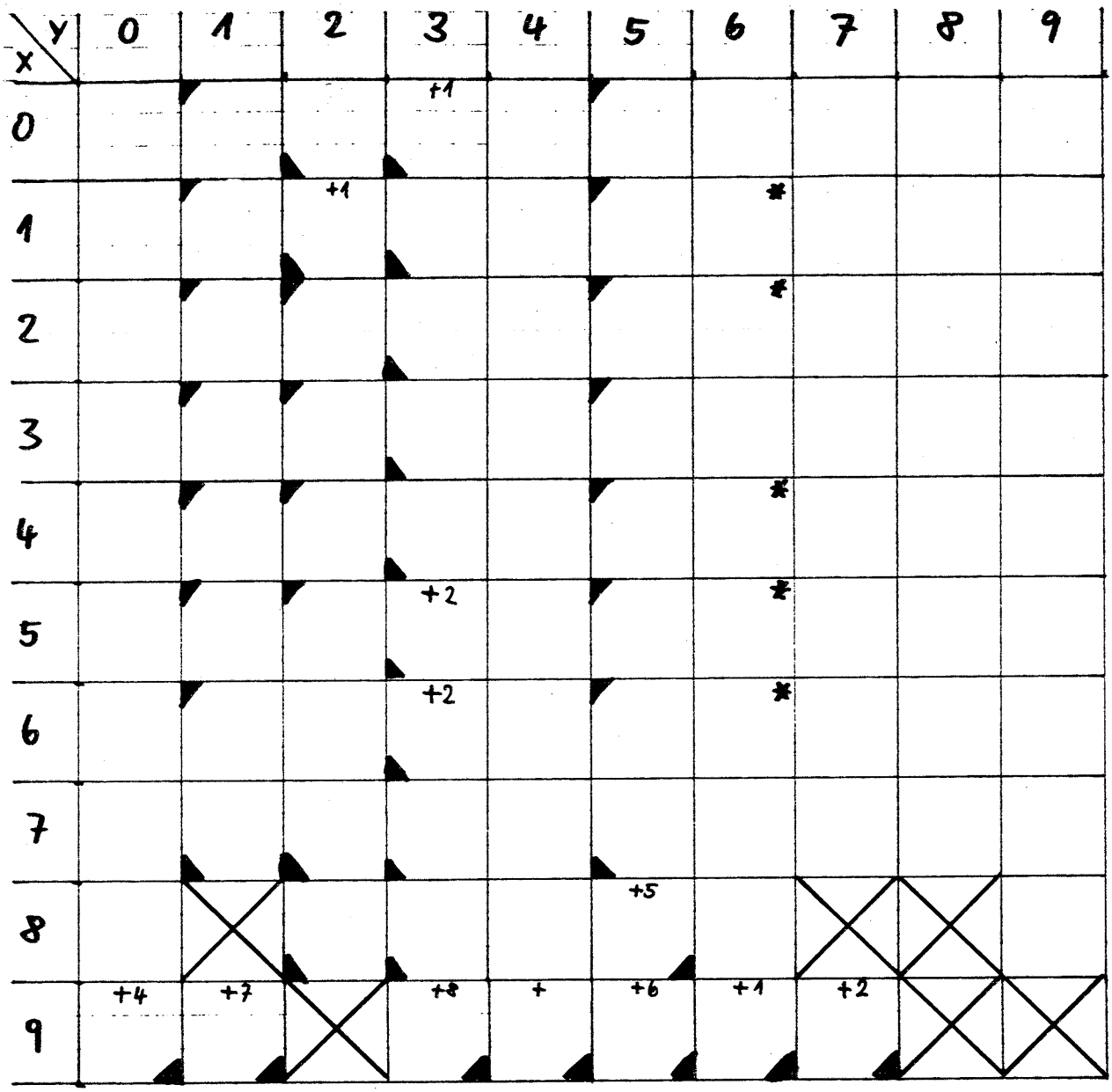
NUM. PAD

CNTR. PAD

ADD. PAD

KEYBOARD MATRIX

MODEL P



+ INDICATOR POSSIBLE
* VIA NAT.VERS. JMP.

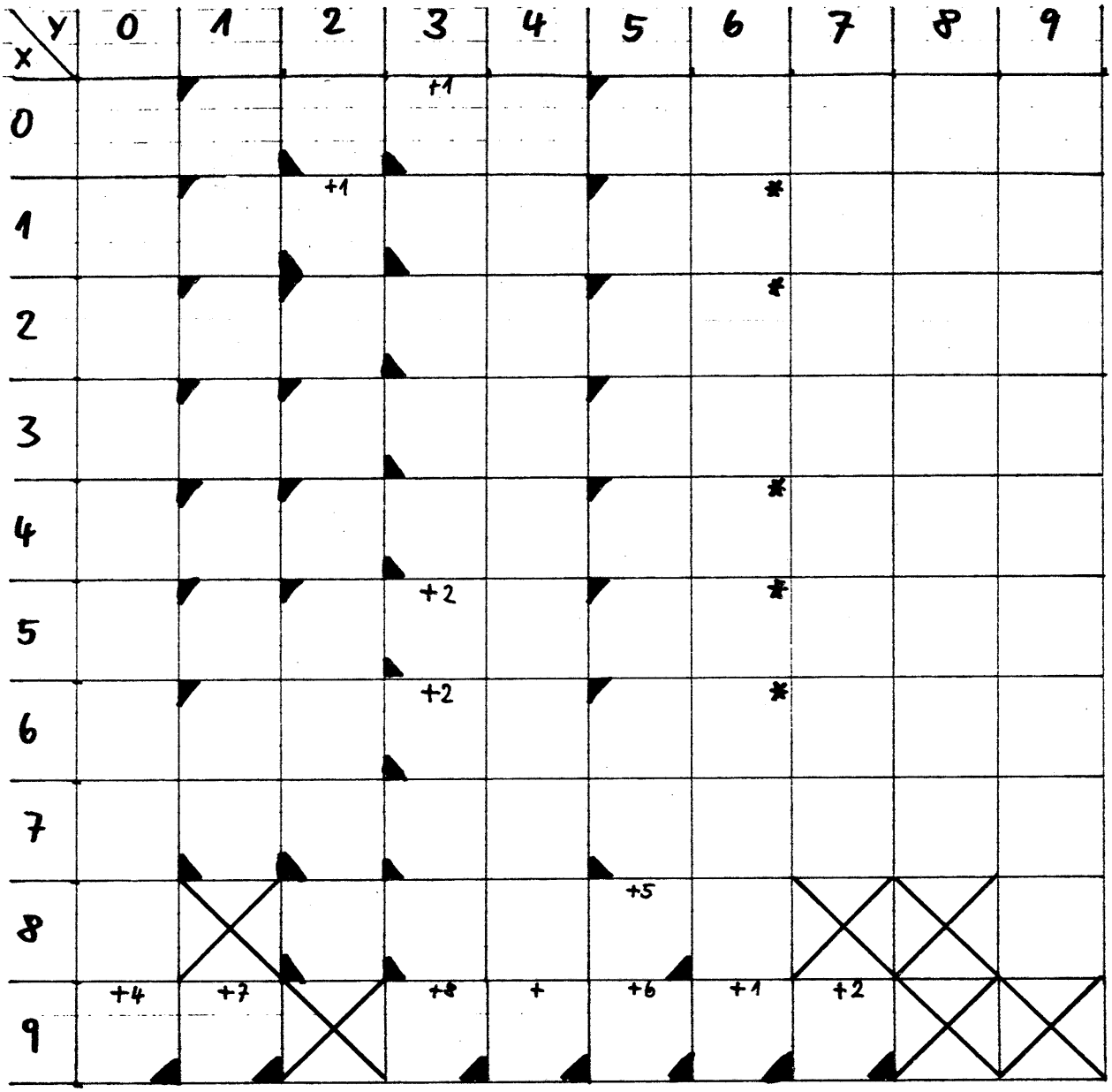
◤ NUM. PAD

◣ CNTR. PAD

◢ ADD. PAD

KEYBOARD MATRIX

MODEL P



+ INDICATOR POSSIBLE
* VIA NAT.VERS.JMP.

NUM. PAD

CNTR.PAD

ADD. PAD

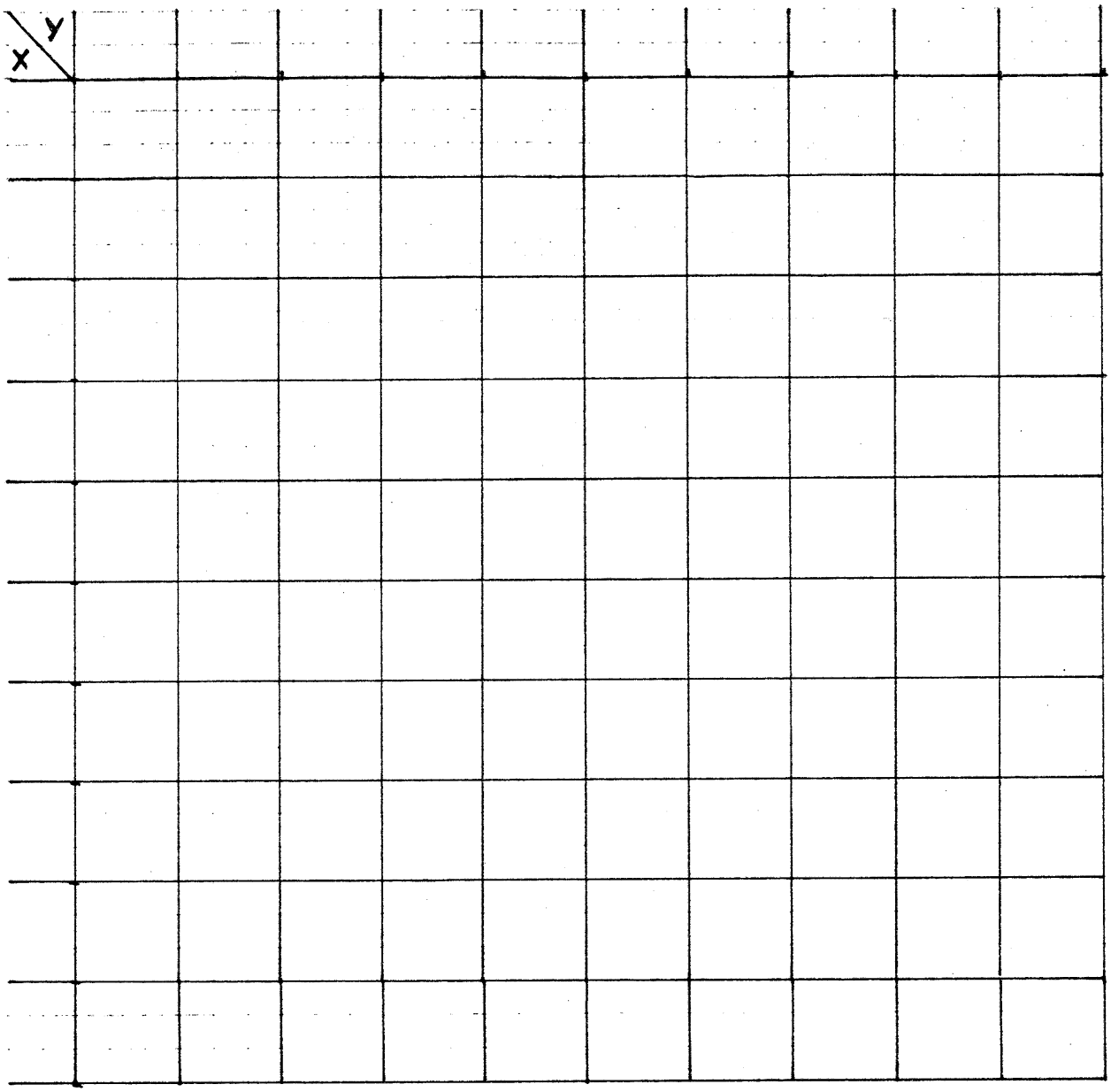
KEYBOARD MATRIX

MODEL P

x \ y	0	1	2	3	4	5	6	7	8	9
0										
1										
2										
3										
4										
5										
6										
7										
8										
9										

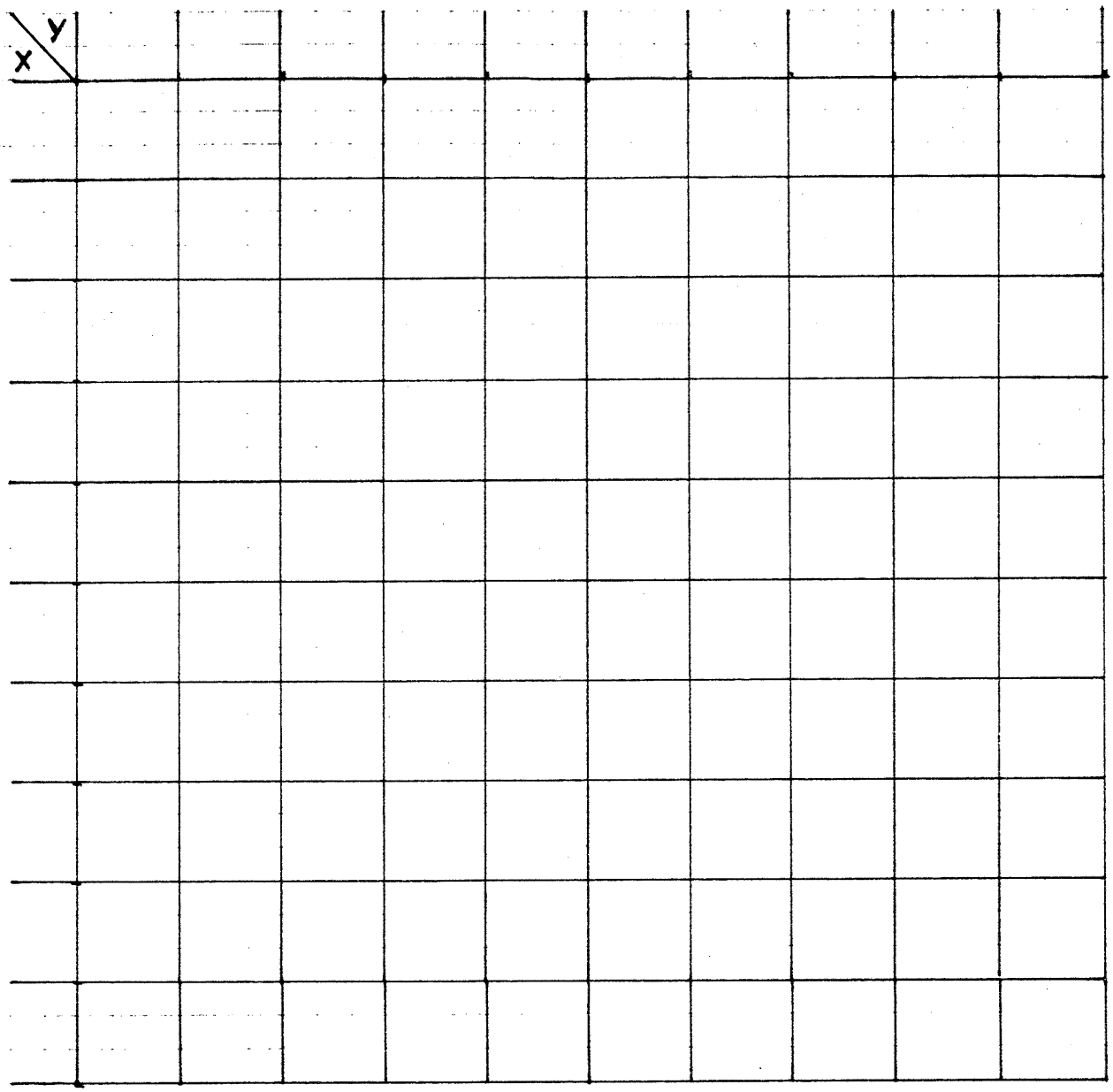
KEYBOARD MATRIX

MODEL P



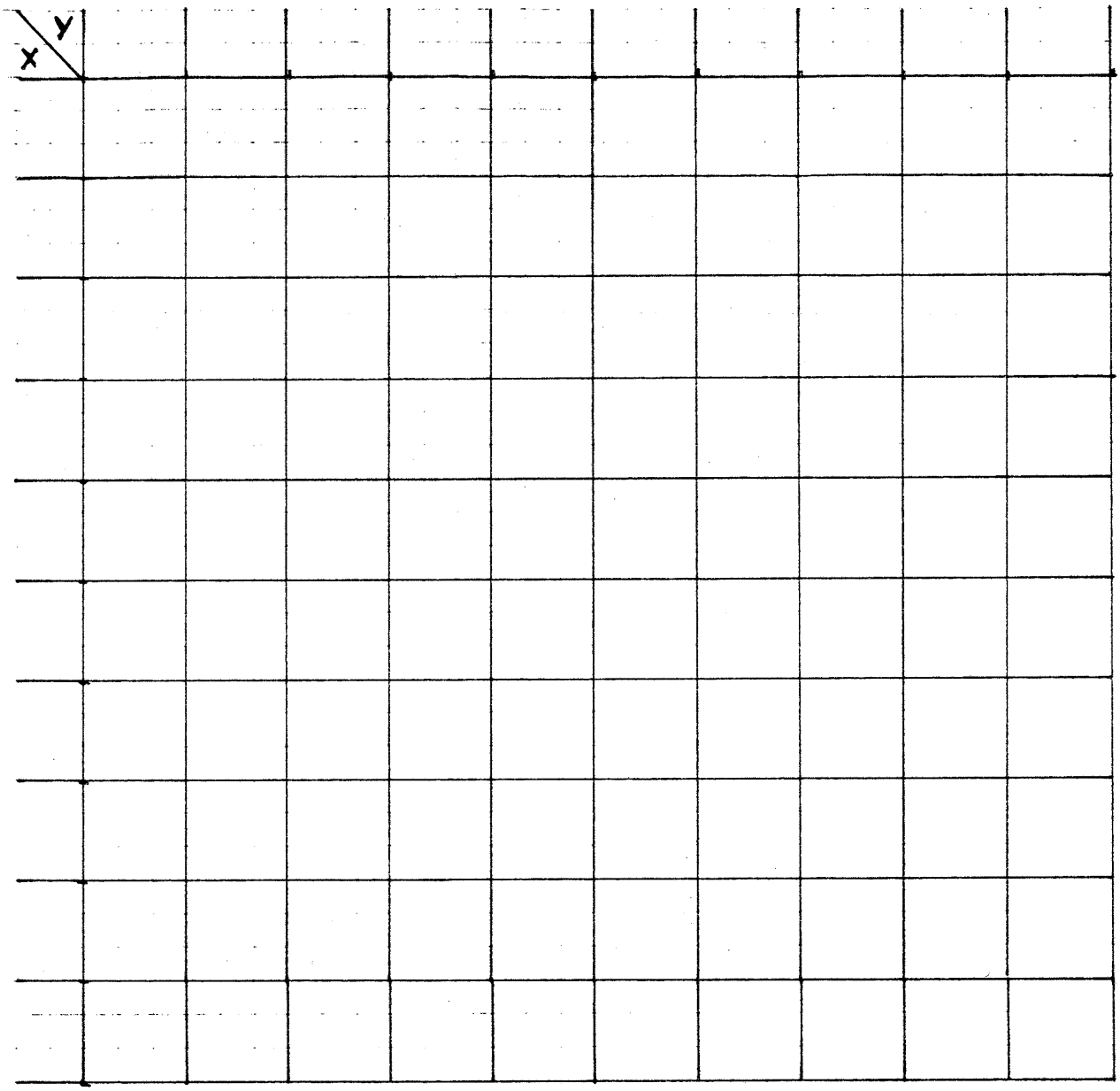
KEYBOARD MATRIX

MODEL P



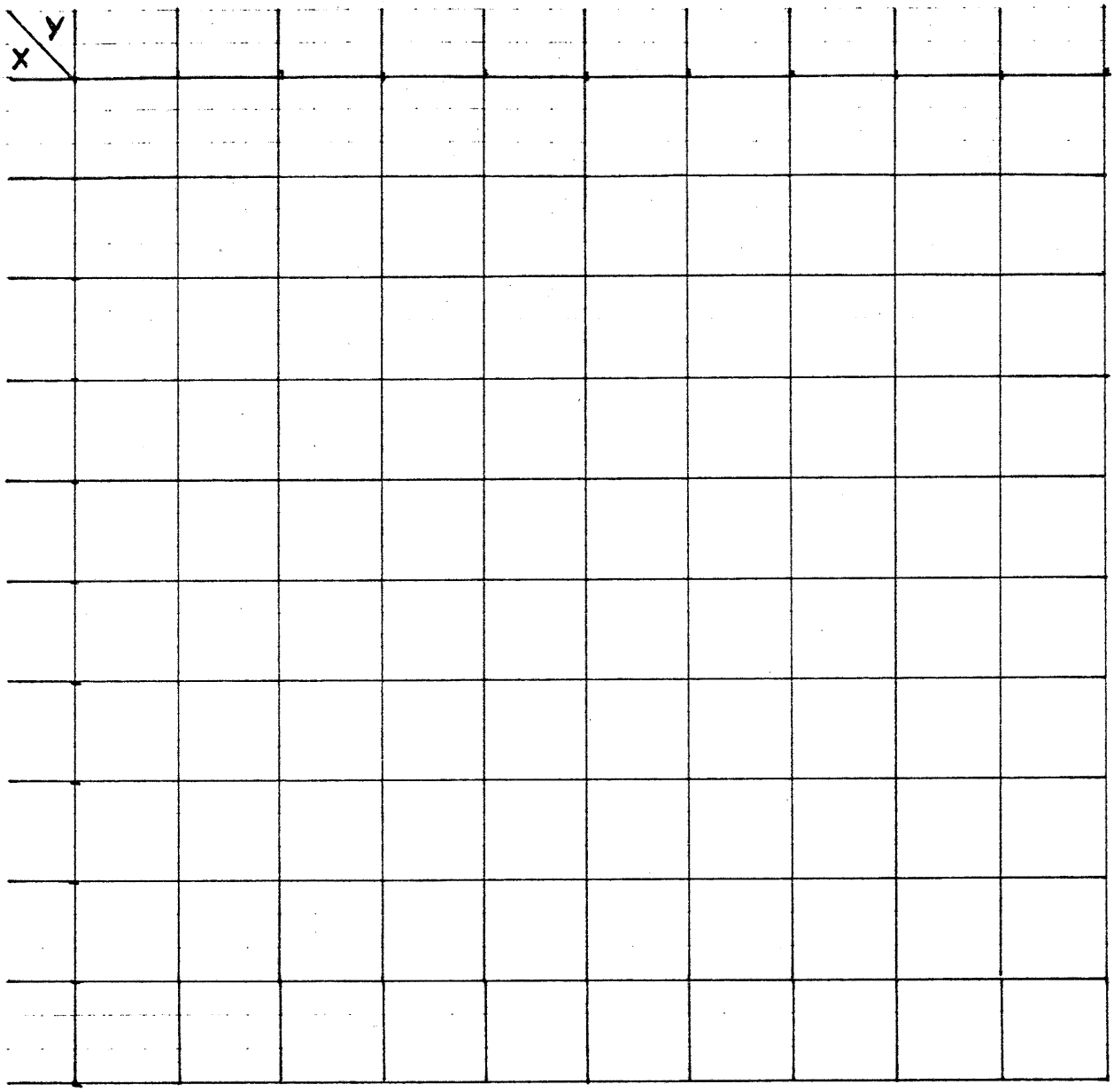
KEYBOARD MATRIX

MODEL P



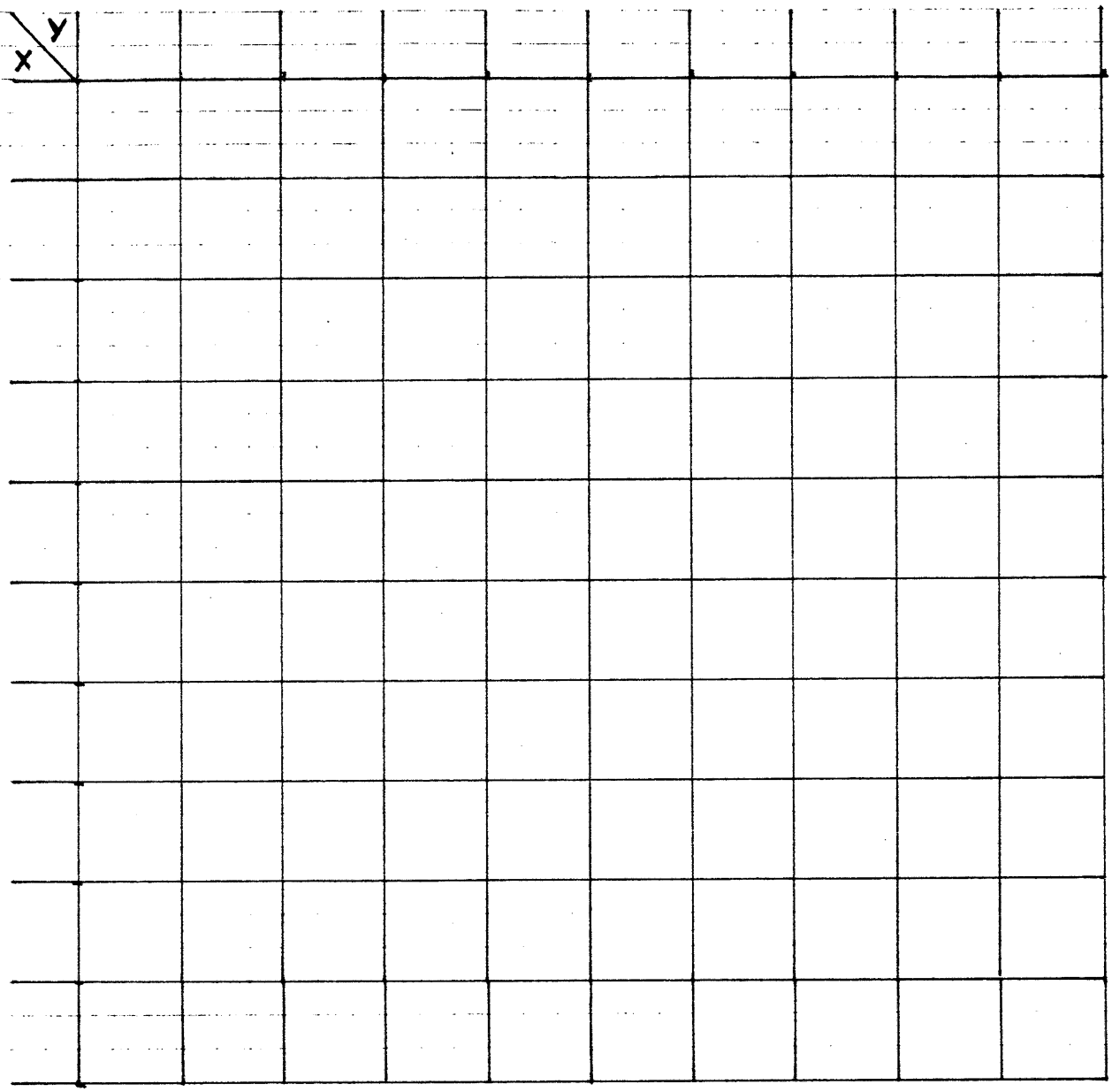
KEYBOARD MATRIX

MODEL P



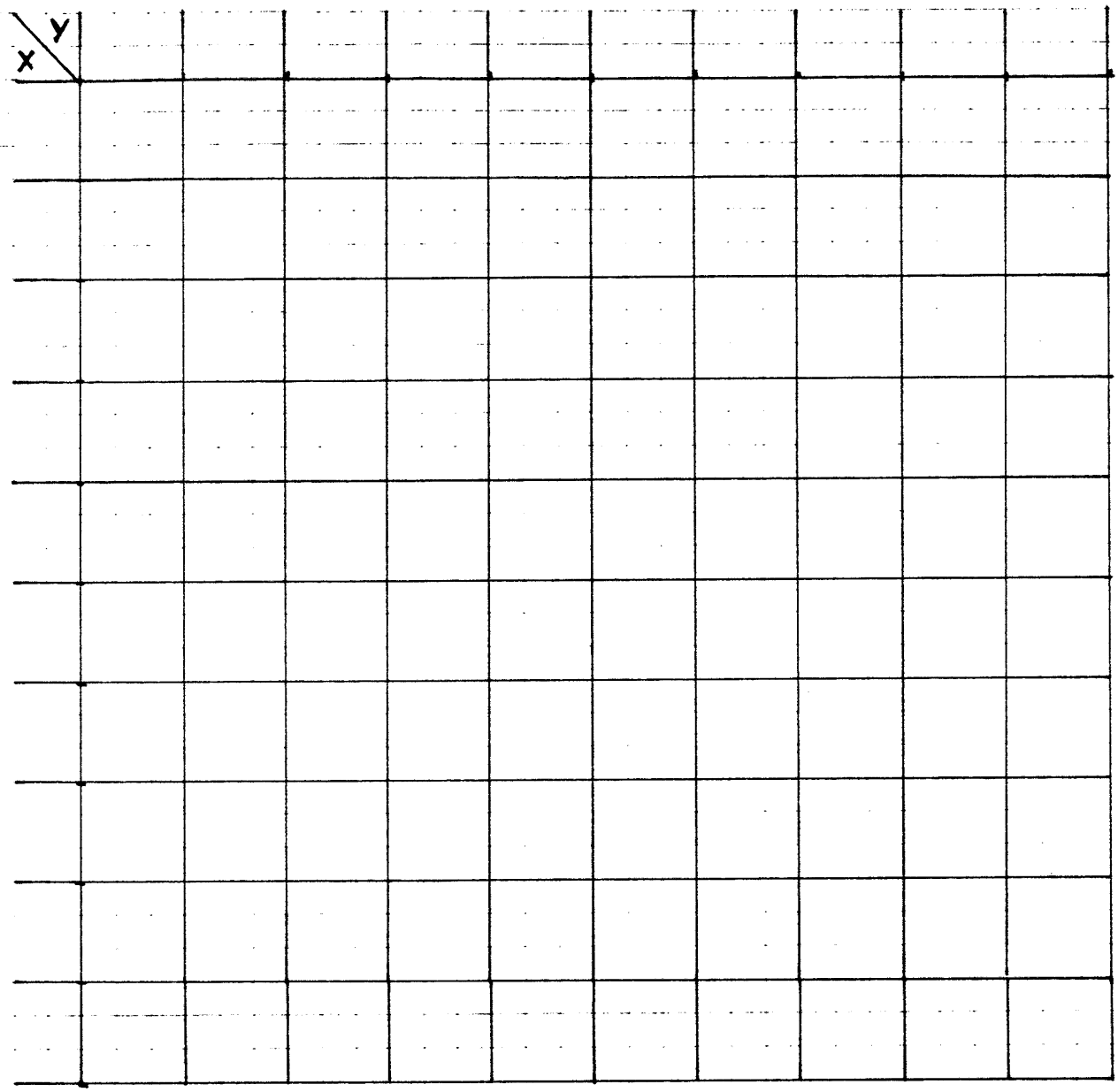
KEYBOARD MATRIX

MODEL P



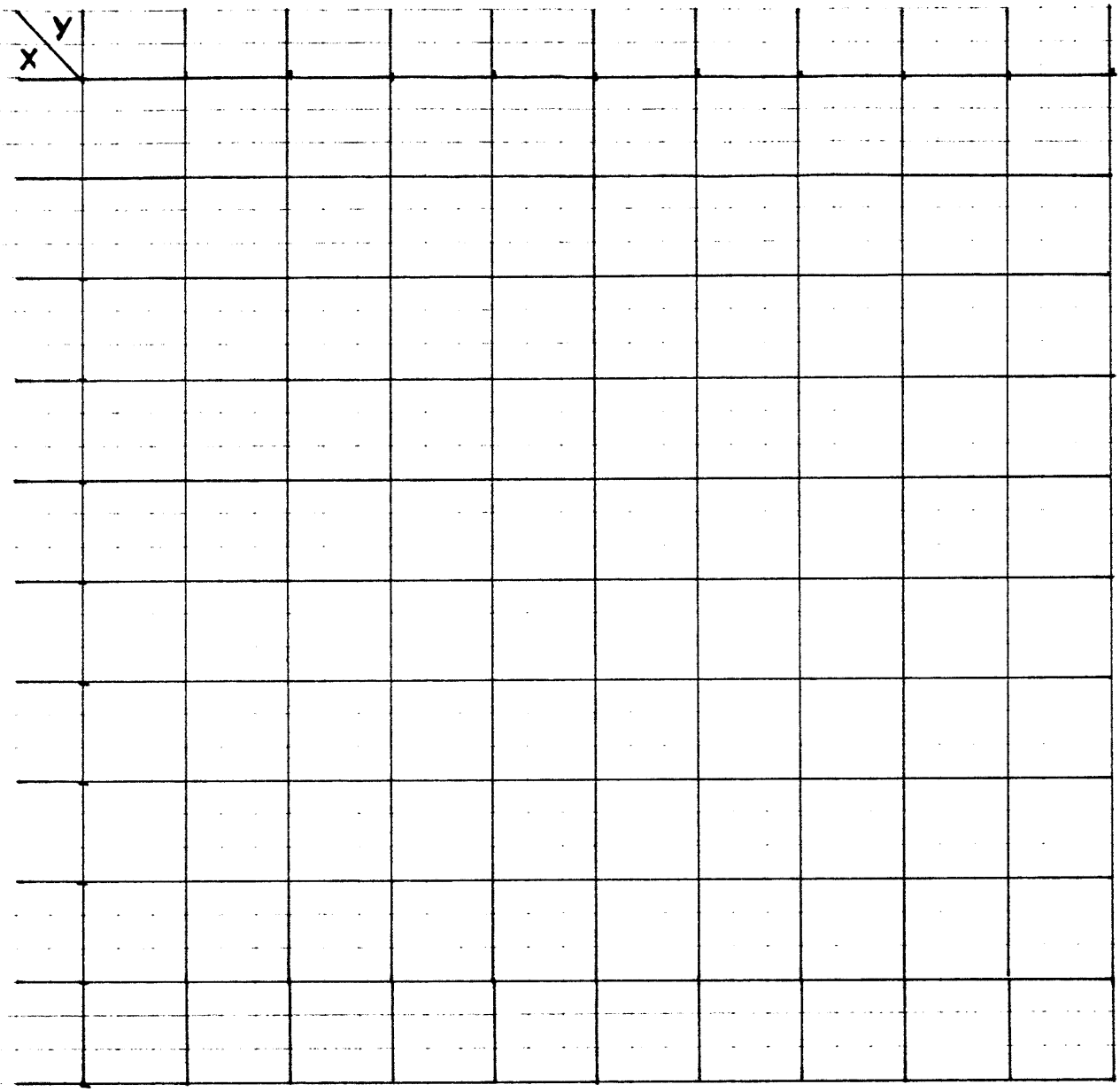
KEYBOARD MATRIX

MODEL P



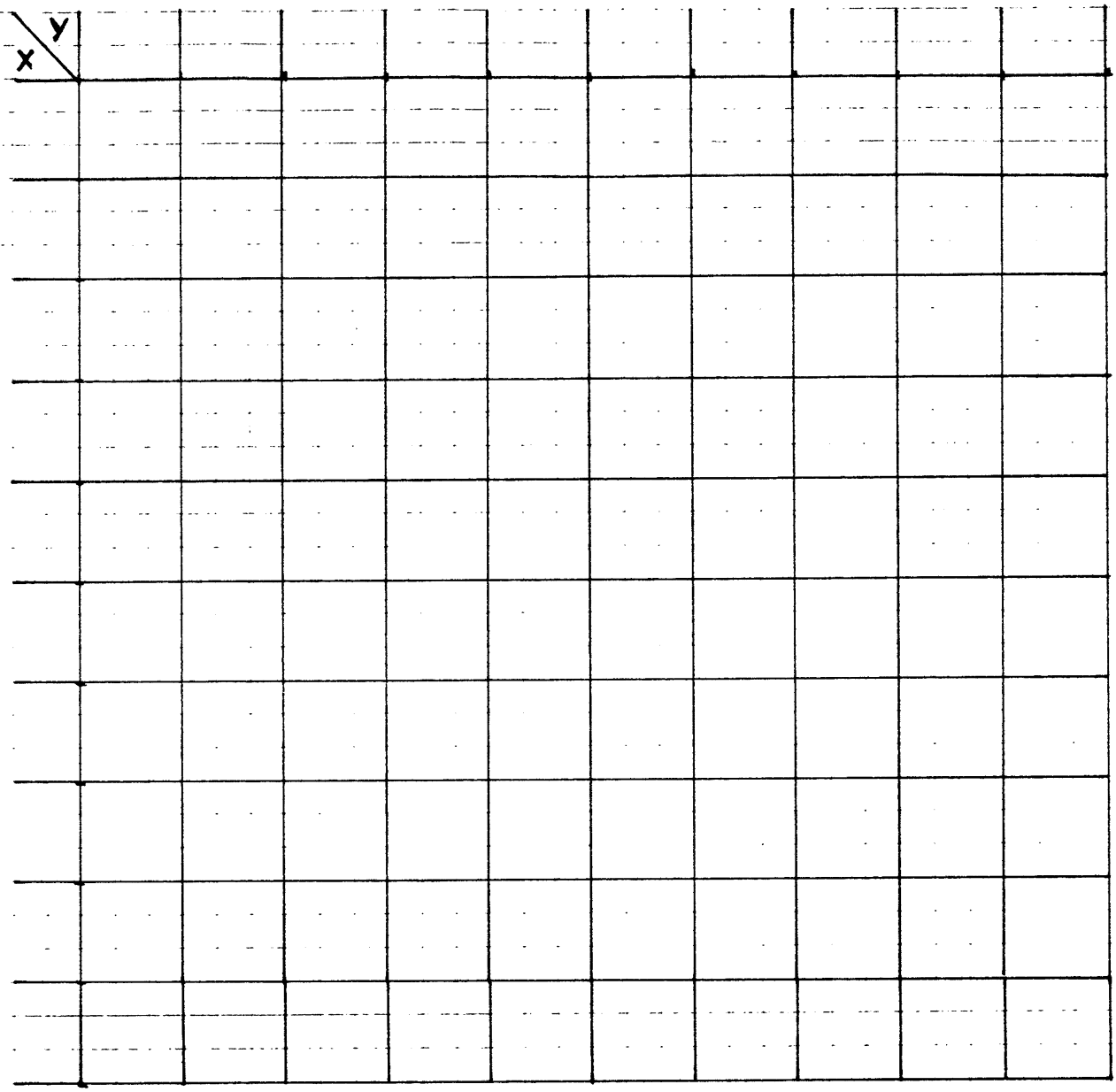
KEYBOARD MATRIX

MODEL P



KEYBOARD MATRIX

MODEL P

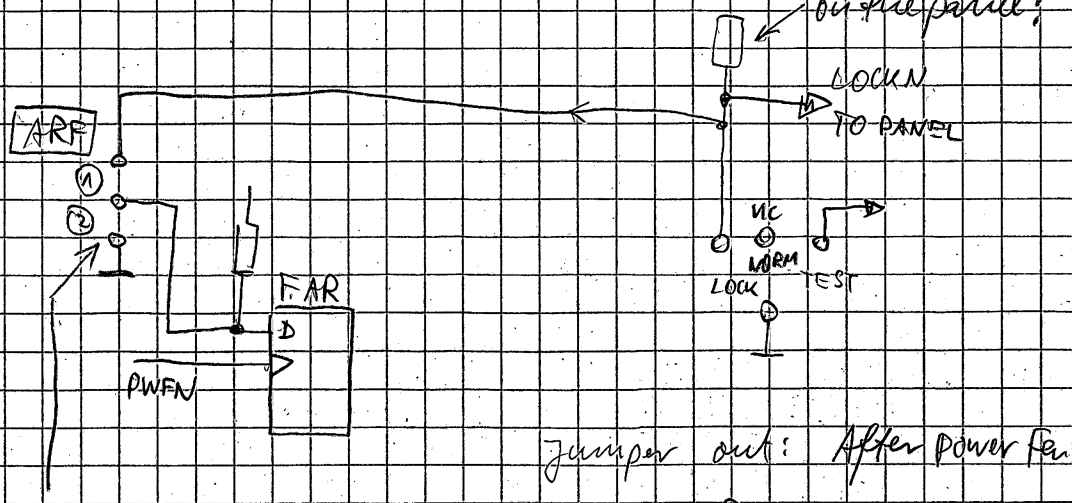


KEYBOARD MATRIX

MODEL P

C-Jen 96441
96451

MP 92971

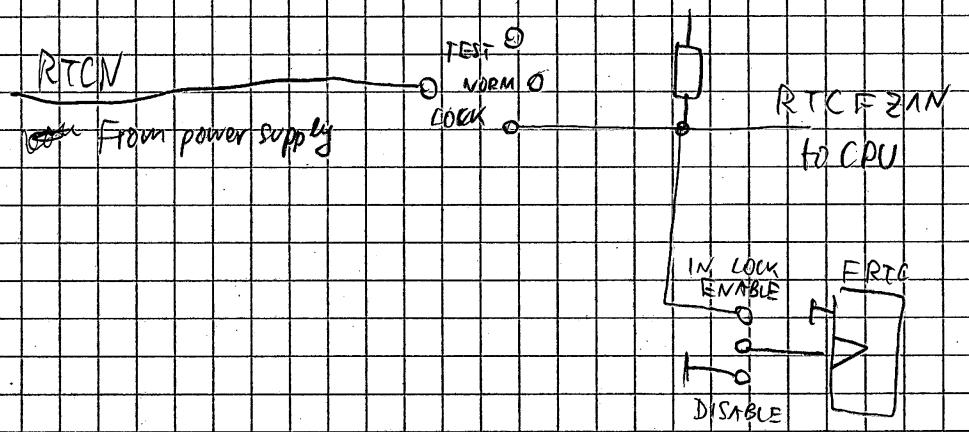


in standard: No pin

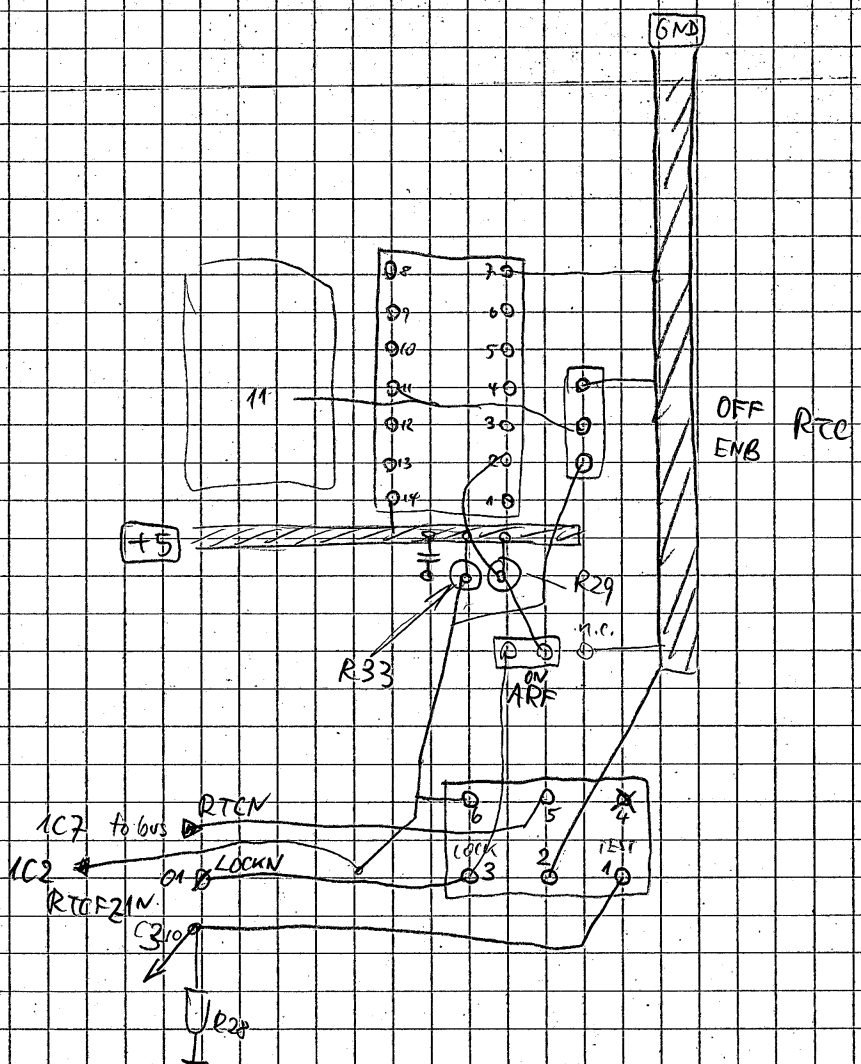
Jumper out: After power fail no Autom. Restart

" ① " " " " Restart, if LOCK

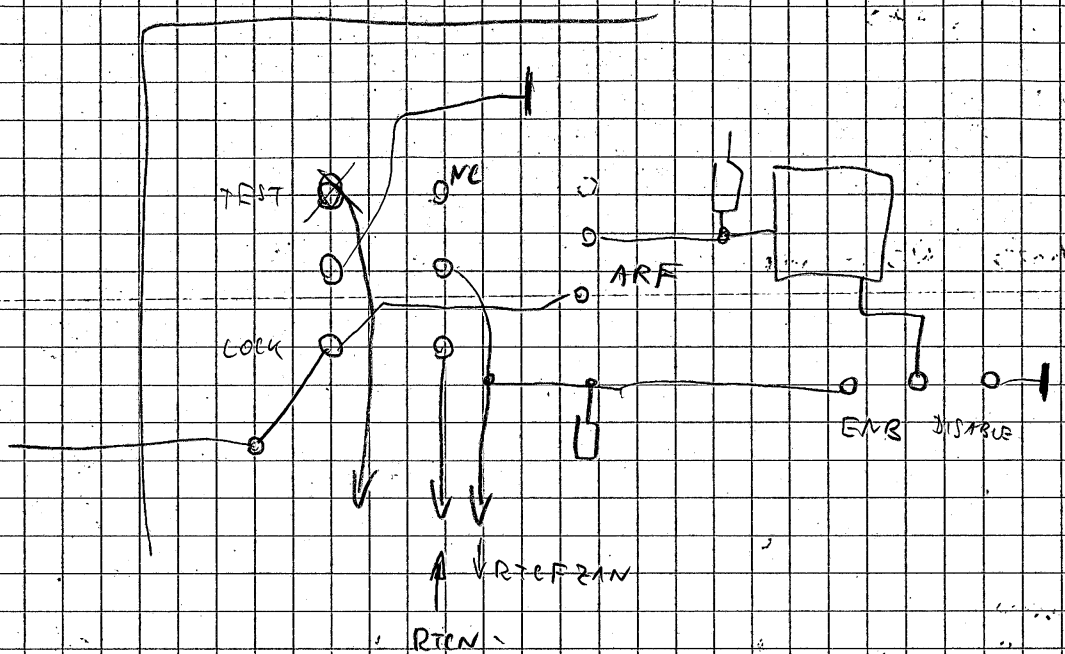
(" ② After pwf always ARF)
(not possible in standard)



If the lock function is not wanted, the switch can be used for RTC/NORM/TEST. To get the function, disconnect the line LOCKN to the panel (solder point 01 on the inter panel


GND
11
OFF
ENB
RTC
+5
R29
R33
n.c.
ON
ARF
1C7 to bus
RTCN
1C2
01
LOCKN
RTCFZIN
C3
R28
LOCK
TEST

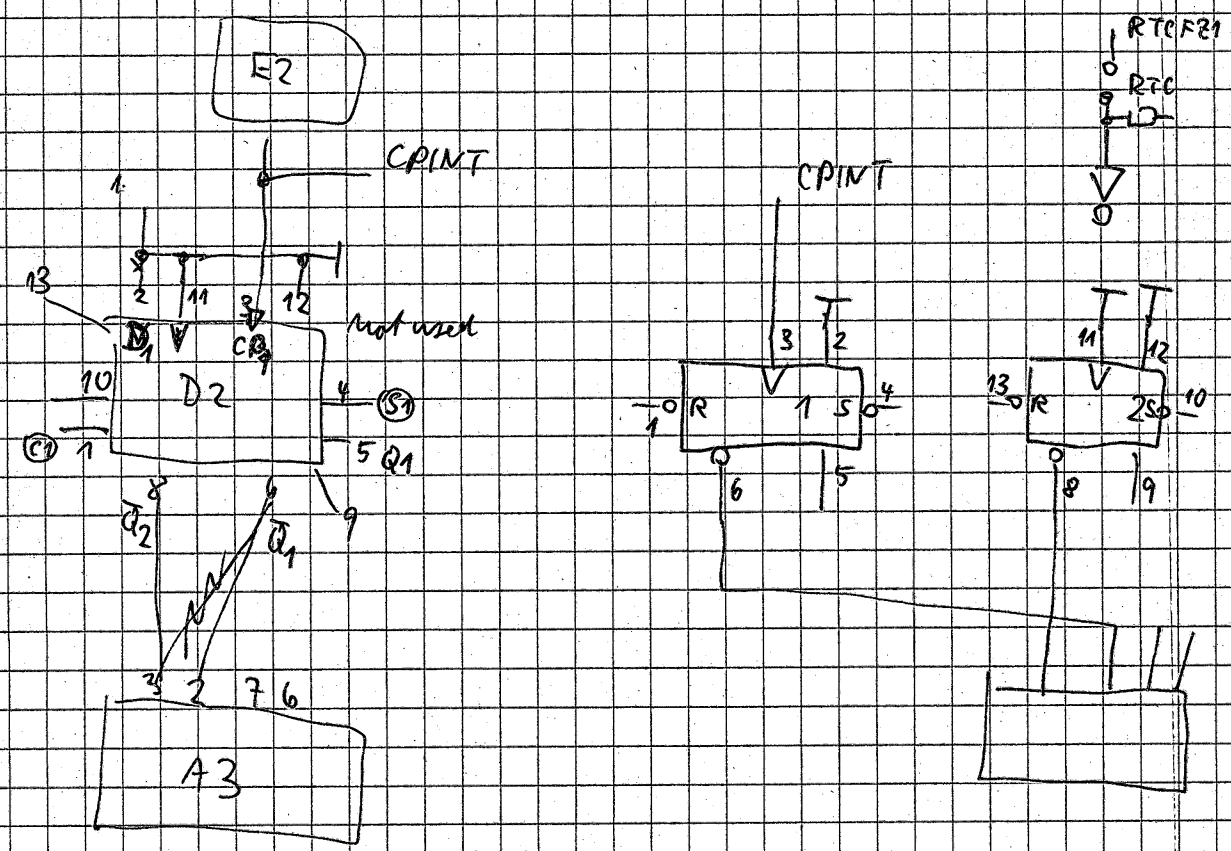
P851



P851

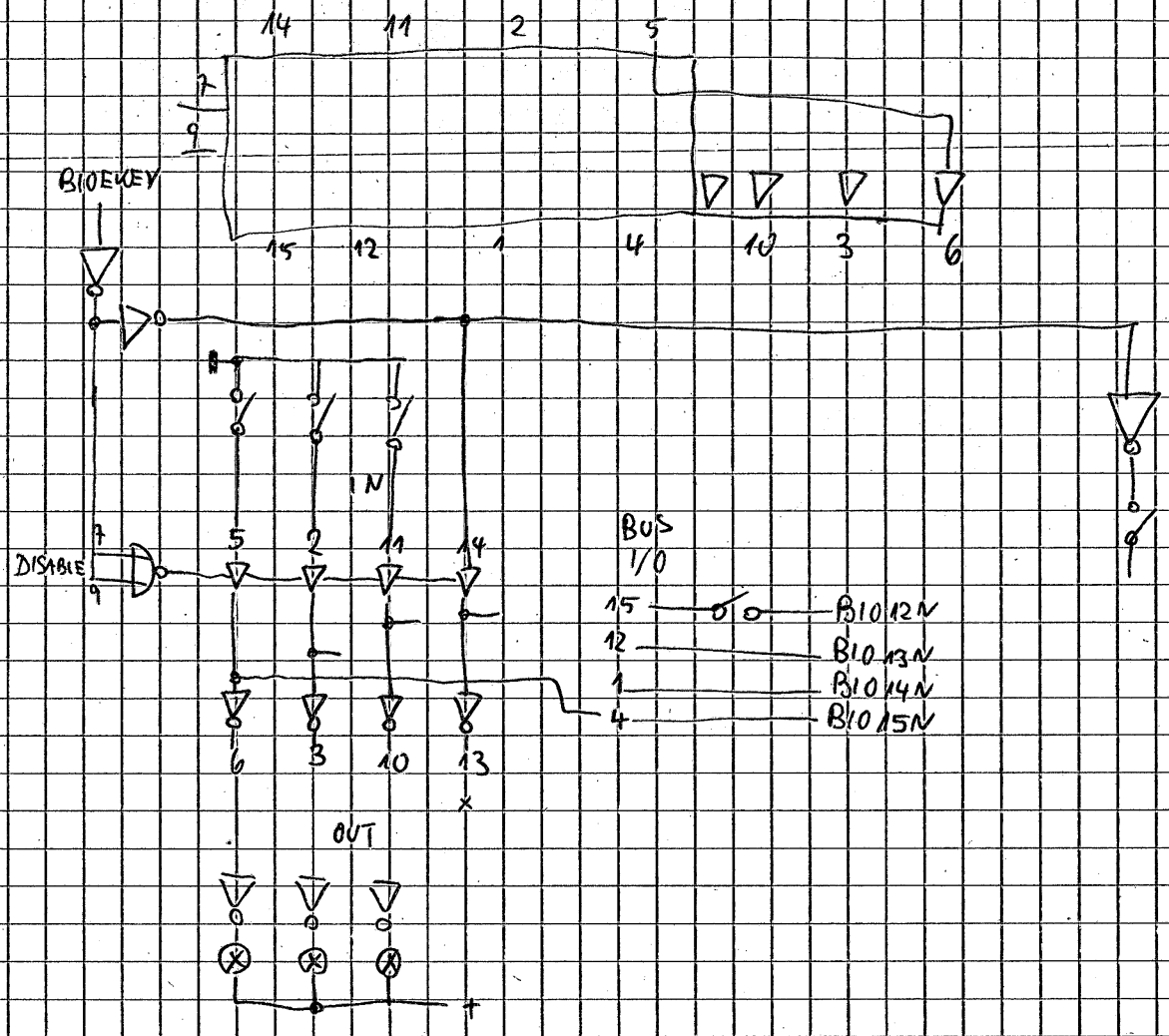
B10

	321
PWF	011
ARF	001
RTC	101
CPI	110
IPL	010
TEST	111

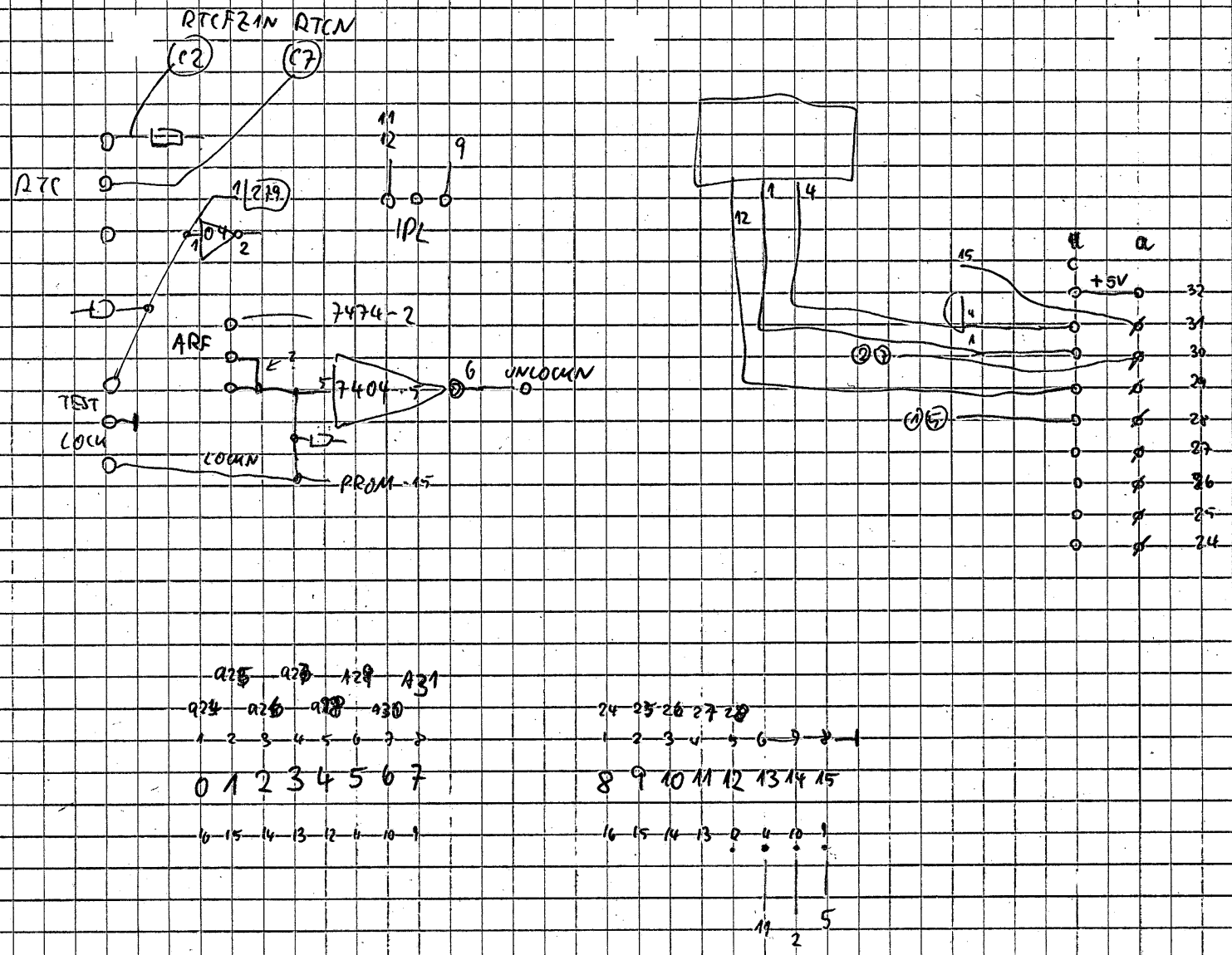


D2

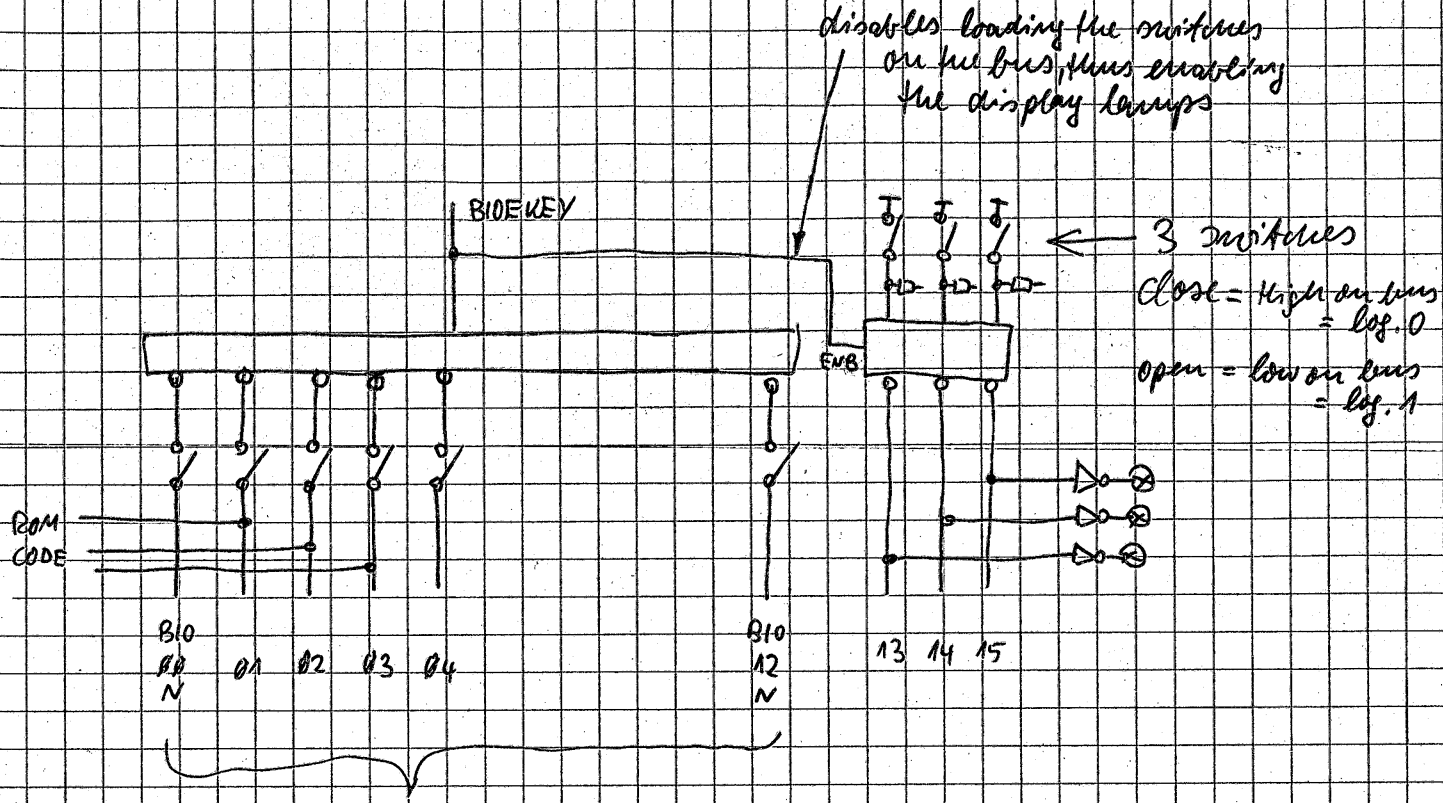
851
INTER PANEL


14
11
2
5
7
9
BIOEKEY
15
12
1
4
10
3
6
IN
DISABLE
7
9
5
2
11
14
BUS
I/O
15
12
1
4
BIO12N
BIO13N
BIO14N
BIO15N
6
3
10
13
OUT
+

PANEL


RTCFZ1N RTCN
C2
C7
RTC
IPL
ARF
7474-2
7404
UNLOCKN
TEST
LOCK
LOCKN
PROM-15
+5V
a
32
31
30
29
28
27
26
25
24
0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15

PANEL



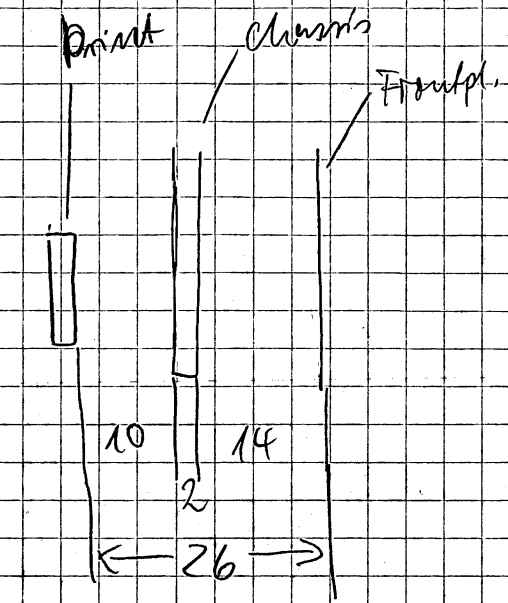
BIO	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
down = ON	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
down = OFF	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

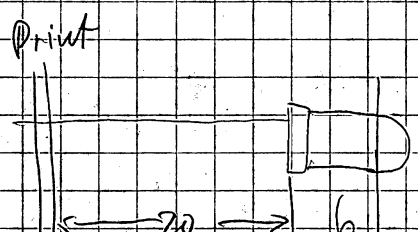
Example:
FD 03
/4083

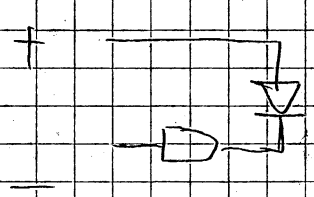
DK 02
/6302

DK 22

PANEL



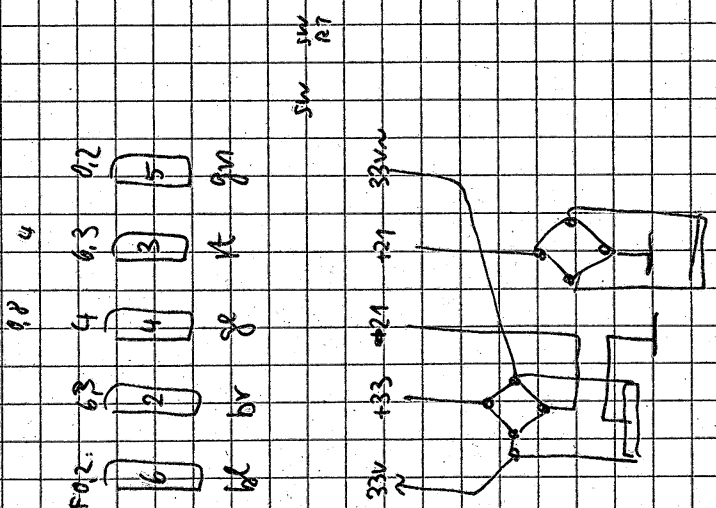




PANEL
LED

Berg-Steuer 6x pro in

Sicherungen B51



Änderung von REG 5V 5111 199 7090 (13A)

neu REG 5VR 5111 199 7088 (15A)

1) Eine Schiebermutter zufügen

2) Sicherungen auswechseln

F3 (alt: D1 4A)

neu: D1 6,3A

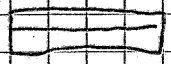
F4 (alt: D1 0,8A)

neu: D1 4A)

3) Regler tauschen

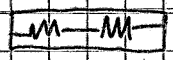
4) 12NC's ändern

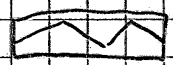
Backpanel	5111 199 7304	3 → 4
Europaer 851	5111 199 7306	1 → 2
Chassis	5111 199 7305	1 → 2



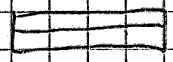


TD T2A

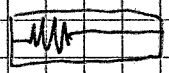




HA21 6,3A



HA21 3,15A



M

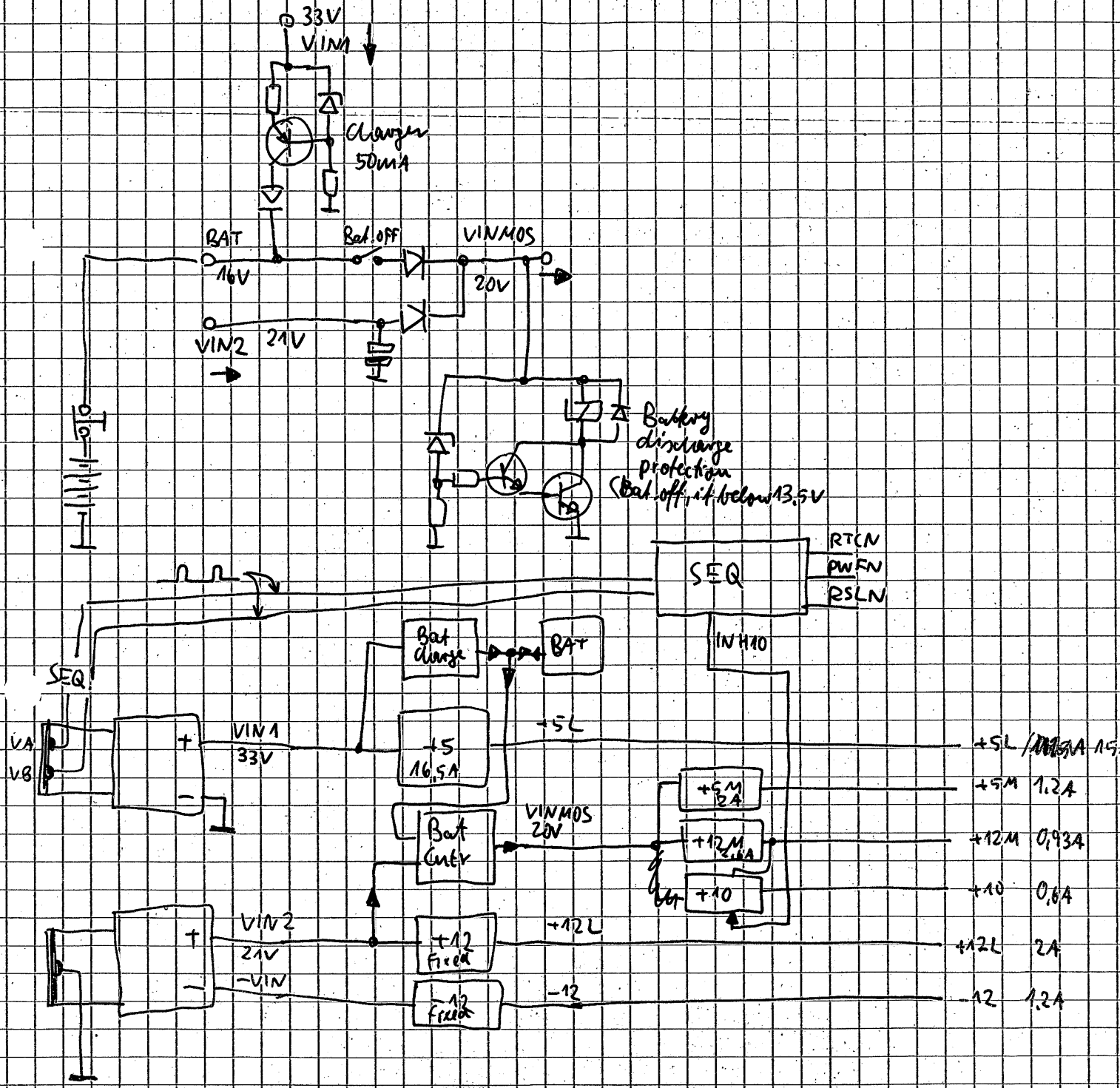
2411 086 0511

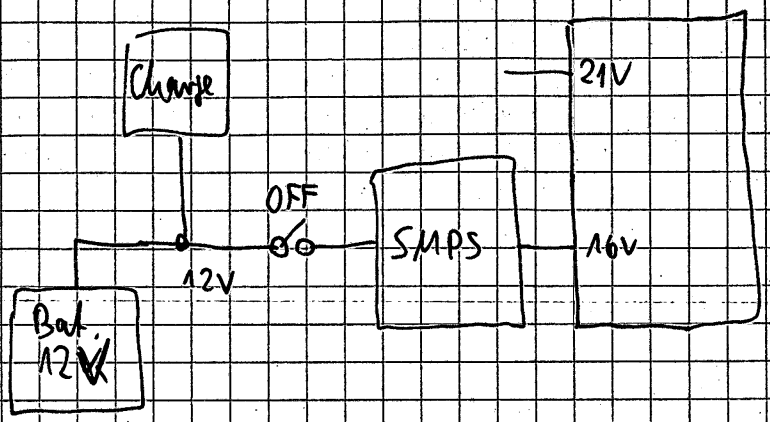
1	0,8
2	
3	
4	
5	4
6	
7	
8	
9	
20	
21	6,3
2	
3	
4	
5	

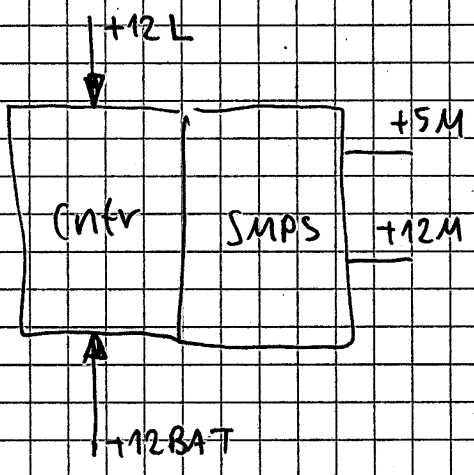
	CPU	MEM	IOP	IOT	BACKP.+CASE	POW SEQ	= ALIMOS	= +5R	= REGT	MINIPAN	FULLPAN	Level	Subj.
4915-16-1										X		1→2	PWF/AR: µP
5733-16-1	X											1→2	AR: µP
" " 2	X											2→3	µP
HSB 38	X												Test tool
40		X										1→2	RAM DZ
44							X						Replacing 134 by 15A
49													Wiring / Grounding
50	X												Bootstrap-Chips
51					X		X						Type label update
1							X	new				→4	OVP
2							X	old				→3	Improvements
3						X						→2	battery
4											X	→4	parasitic pulses
5										X			RTC spurious
6													Battery condition
7							X					div.	Modifications
8		X										3→4	access at pon
9	X											ms	internal interrupts
10							X					new ME	Blocking
11							X					→2	trigger
12										X		→3	Compat. HHP
13					X							→5	" "
14							X					new dev.	Oscillation
15		X										→2	oscillator
16	X											→4	Blocking of bus
17						X						→2	Mem. voltage
18		X											New PROM-card
19										X		→2	new layout
20										X		div.	open inputs
21							X					-3	dropping
22							X					-3	" "
23										X		div	Start-problem
24													6U6-chassis
25	X											4→5	blocking
26													6U6-chassis
27													
28													
29													
30													

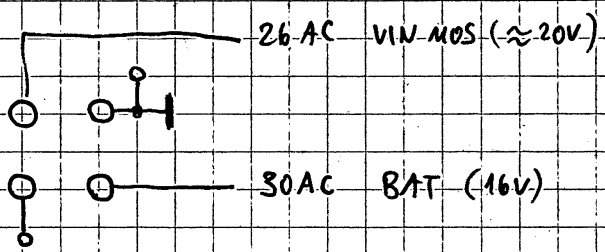
4 Wo gen.

0.5
250K



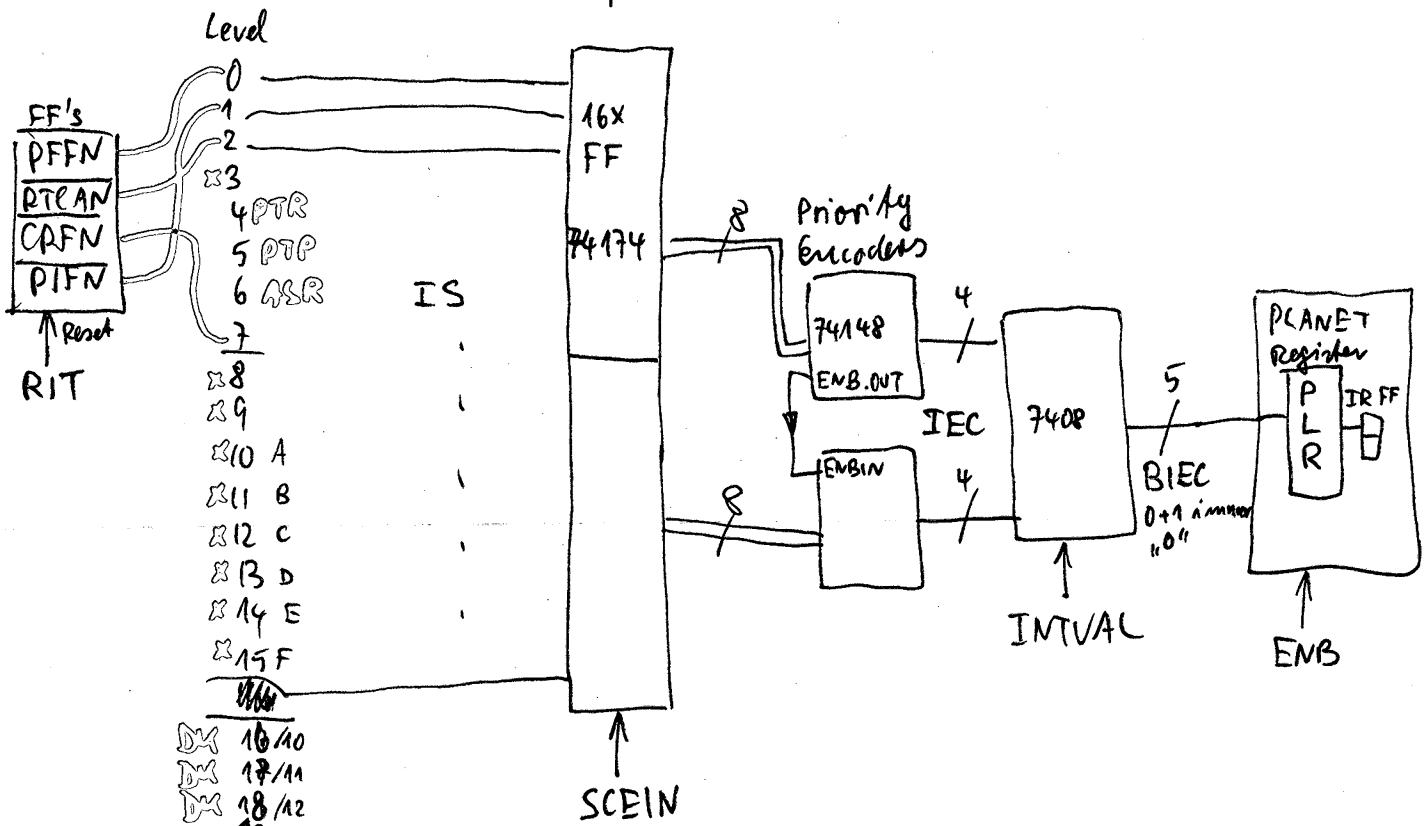

Charge
21V
OFF
SMPS
16V
12V
Bat.
12V

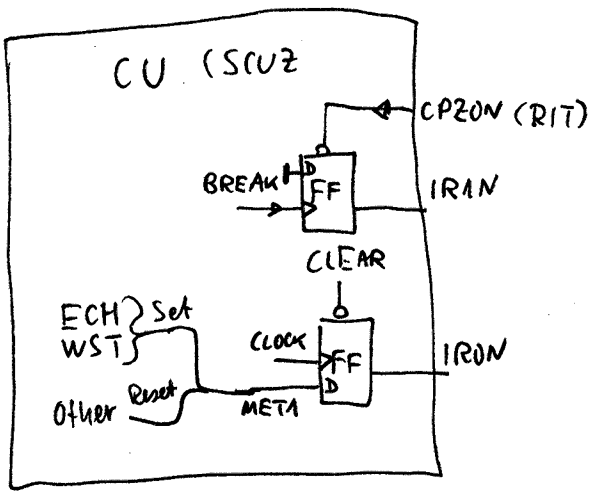

+12 L
+5M
Cntr
SMPS
+12M
+12BAT


26 AC VIN MOS (≈20V)
30 AC BAT (16V)

Sponsel

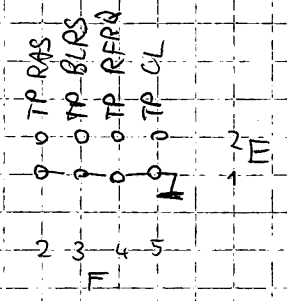
P-851 Interrupt

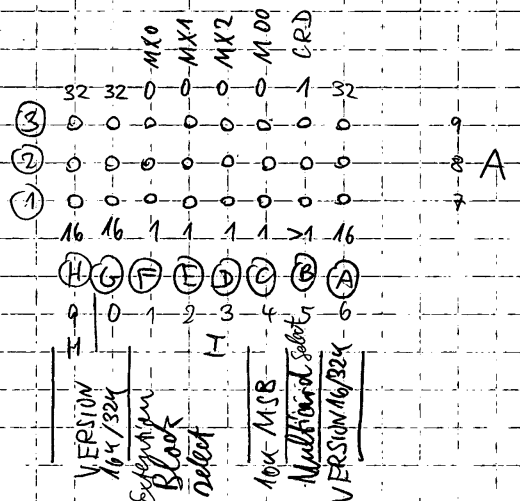


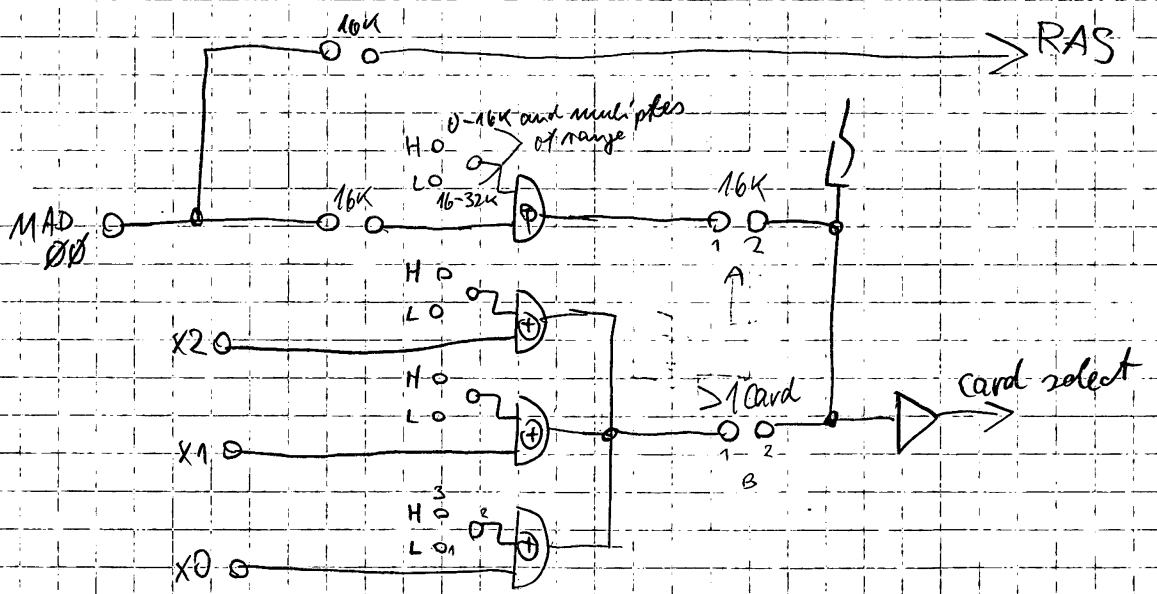


63 CPU IDLE

P851
IR-System


TP RAS
TP BLRS
TP RFRQ
TP CL
2
1
E
2 3 4 5
F


MX0
MX1
MX2
MOD
CRD
32 32 0 0 0 0 1 32
3
2
1
9
8
7
A
16 16 1 1 1 1 >1 16
H G F E D C B A
9 0 1 2 3 4 5 6
H
I
VERSION 16K/32K
Extension Block select
10K MSB
Multicard select
VERSION 16/32K


16K
RAS
0-16K and multiples of range
H
L
16-32K
MAD ØØ
16K
16K
1 2
A
H
L
X2
H
L
X1
>1 card
1 2
B
card select
H
L
X0

GMA1

BRAM
PV X52-126

RAMDZ	4/8K	P851	RA4/RA8
GMA1	16/32K	"	RA16/RA32
M8/16/32H		852,6,7	
M32E		857	

Load stop /0200

Default: Check 0...8, 10, 10.1 (check 9 is option)
Testing from end of program to 32K
Stop on error (/0100)
Stop after one cycle of all checks (/0200)
(chip type must be loaded)

IR0 = PWF
IR1 = LUM
IR2 = RTC

A9

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	1 = 4K1 chip	1 = 16K1 chip							1 = No stop at end (loop)	1 = No stop at error					

A10 Check Numbers
A11 ~~Start~~ Begin address first addr. to test (071C)
A12 Last " " " (FFFE)

General remarks on Euro-memories

1) RAMSZ:

Only one card of this type possible, being bottom of memory. No combination with other memory types useful, smallest fraction of other types is 4K with RAMDZ, so a gap of 2K would result.
Only useful for special applications.

2) RAMDZ:

Old standard memory for P851. 4K and 8K modules may be mixed but attention to avoid overlapping of address ranges. Because of power supply limits a maximum of 4 cards should be used. Mixing with EPROM modules possible.

3) GMA1:

New standard memory for P851. In case of 32K module no other memories may be added, other 32K-modules only in extention mode (not possible in P851), 16K-modules are mixable with other types.
Extention mode allows the selection of up to 16 cards of 16K resp. 8 cards of 32K, giving an address range of 256K words. This is a pre-stage of extended mode in UPC-Systems.

Memory Test program for dynamic RAM: BRAM

(tests RAMDZ and GMA 1 below 32K)

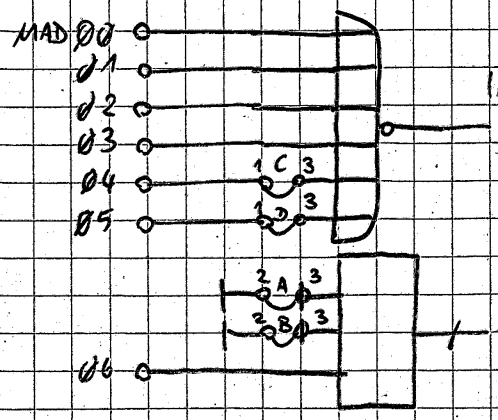
checz	0	„0"-pattern	5	characters
	1	„1"-pattern	6	Row access
	2	word address	7	Column access
	3	char. address	8	Butterfly RAMDZ
	4	words	9	Ping-Pong
			A	Butterfly GMA1

Tests 0...5 are standard
Tests 6 & 7 are only executed in higher part of memory, if no auxiliary memory is available
Tests 8 or A depend on used chip type
Test 9 is optional, it takes ≈ 22 min to test 4K!

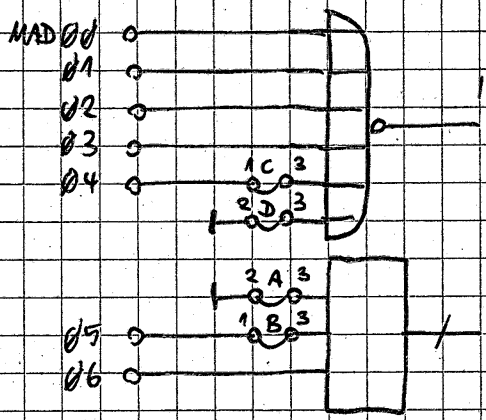
Before starting the program, some registers have to be set:

A9: bit 0 = 1 for RAMDZ, bit 1 = 1 for GMA1 (def. = 0)
A10: checks to be run (def = /FFA0)
A11: lowest tested address (def = /0710)
A12: highest tested address − 1 (def = /FFFE)

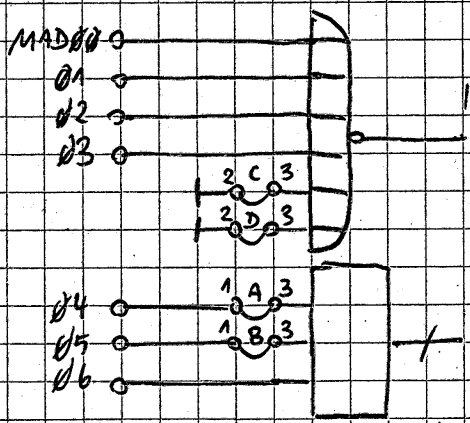
If errors are found, certain registers will have to be read.



0,5K module



1K module

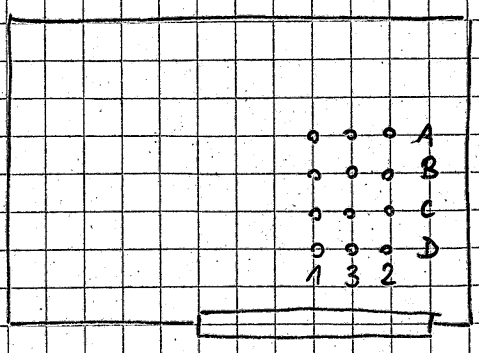


2K module

Jumpers factory installed, soldered corresp. mem. size.

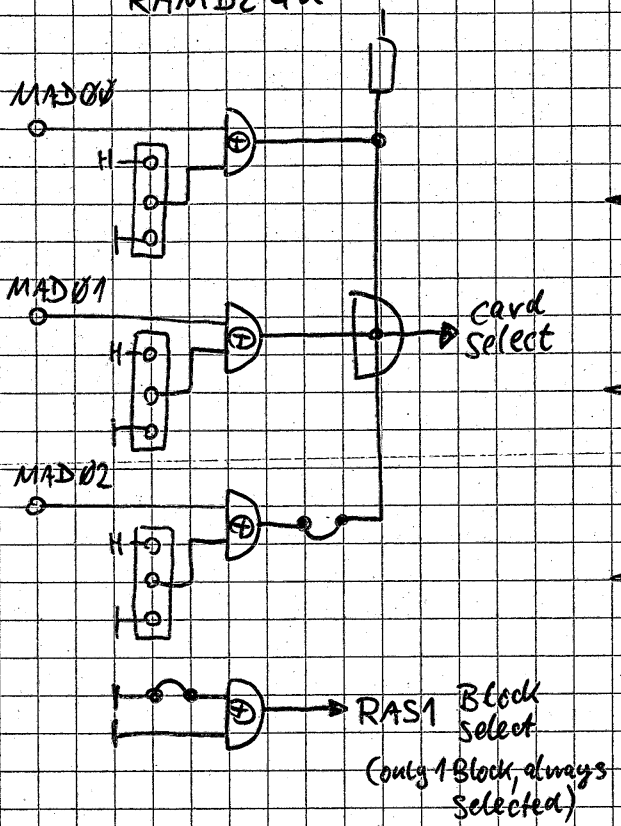
Addressing always starting at 0 (card is RAM bottom)!

Only one card per system!

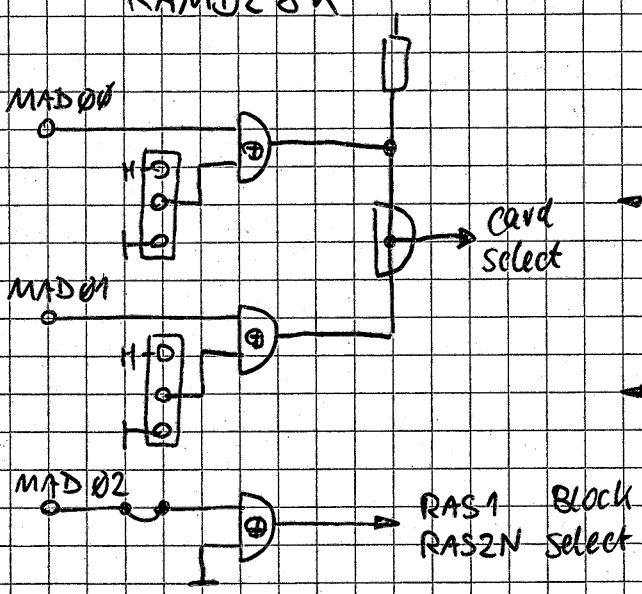


RAMSZ

RAMDZ 4K



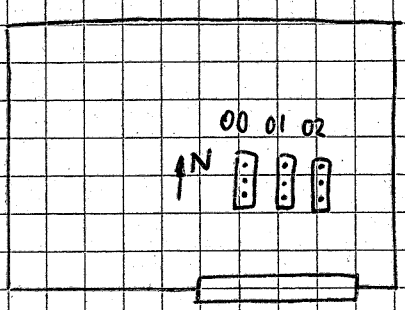
RAMDZ 8K



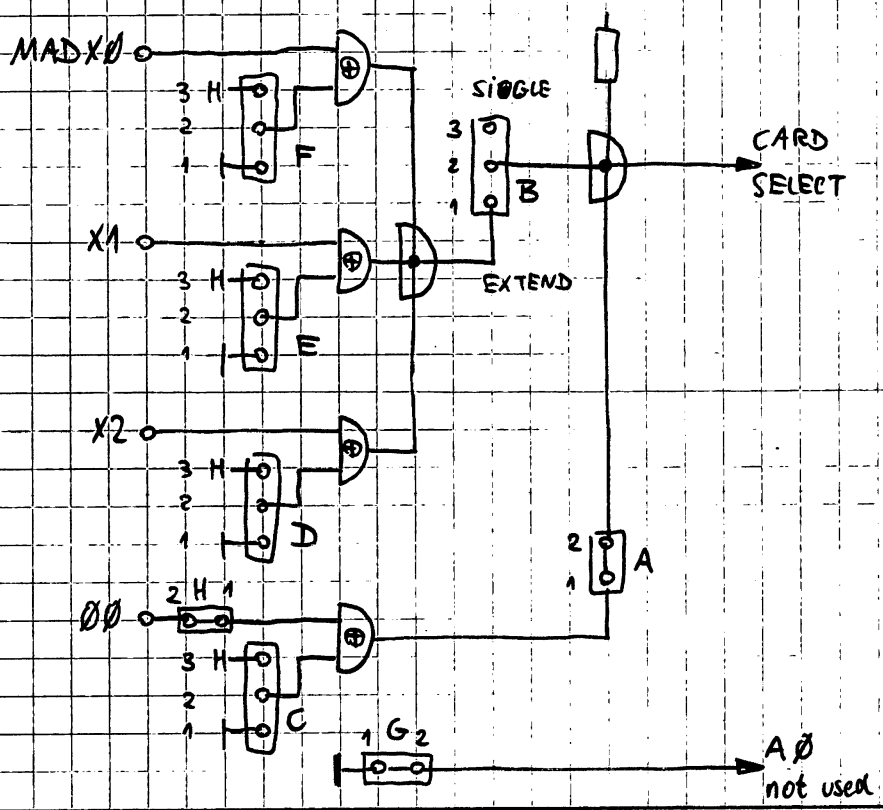
Factory solder jumpers

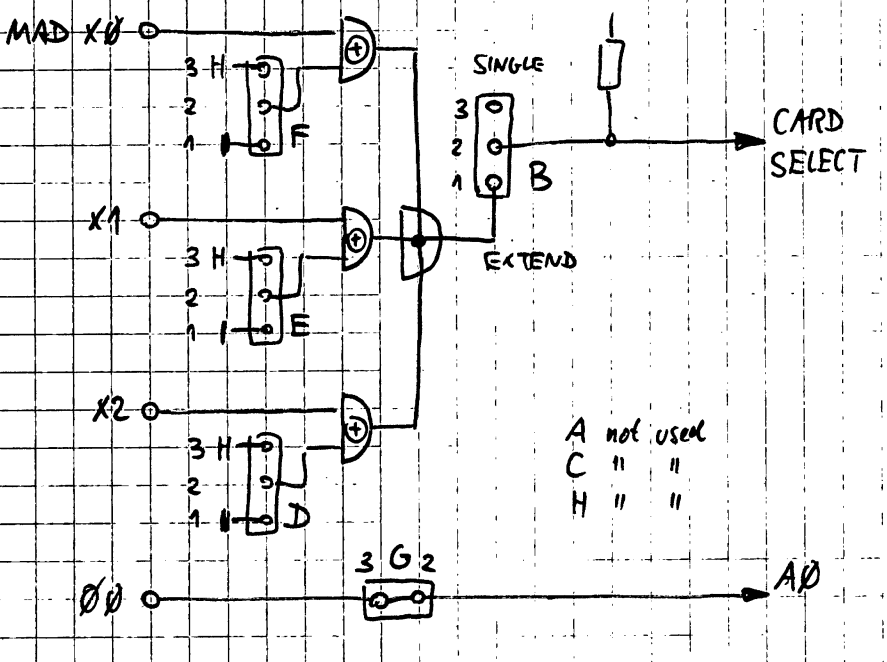
Jumper plugs

(all up: lowest addresses)



RAMDZ



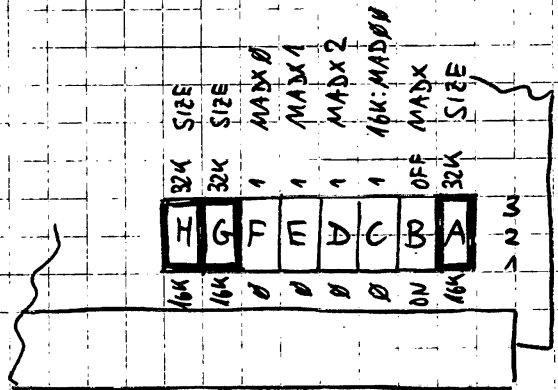


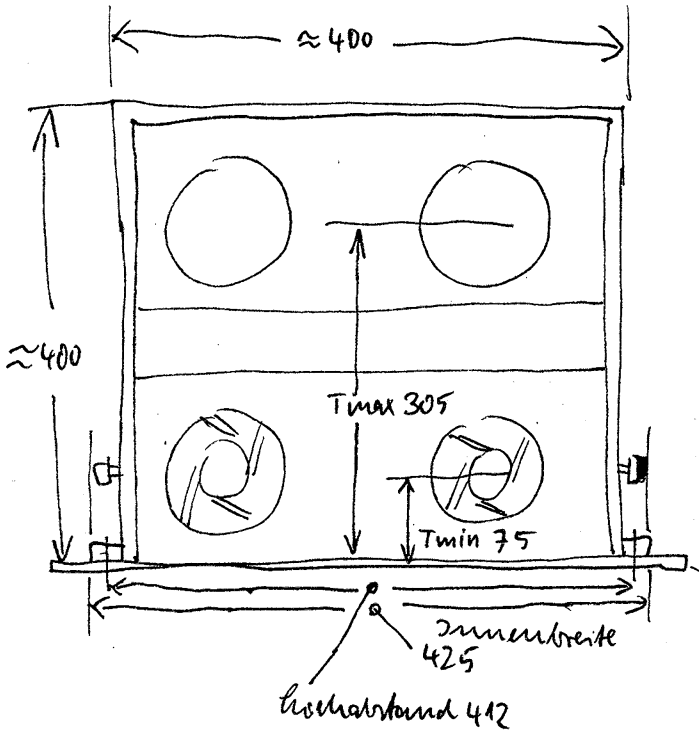
Jumpers A, G, H Factory installed

Jumper C not relevant for 32K

Jumpers D, E, F not relevant if jumper B not = 1 (on)

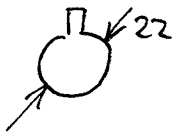
not relevant jumpers: set to 3

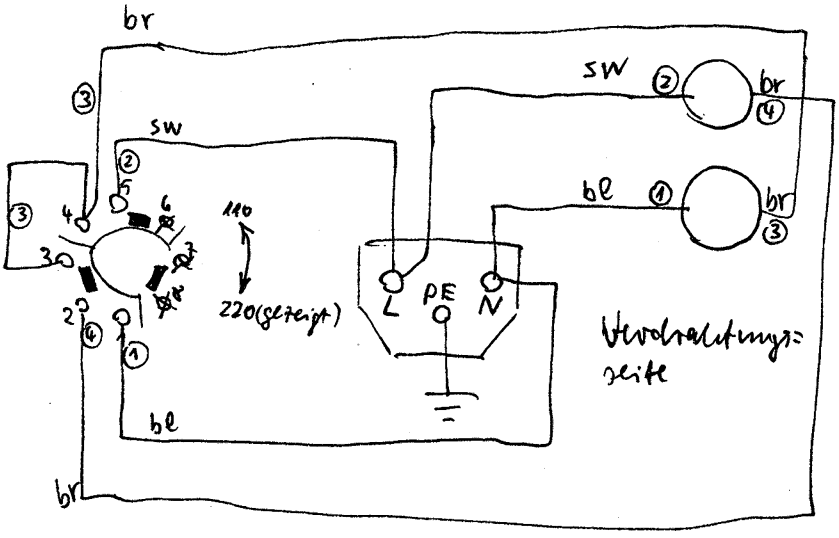


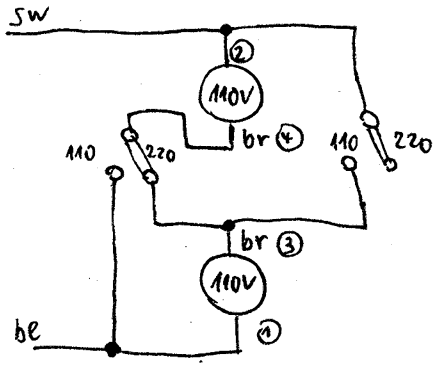


Lüftereinschub
PC 1053/00

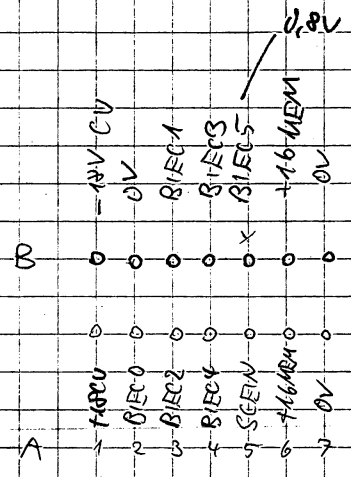
Bohrung Spannungswähler



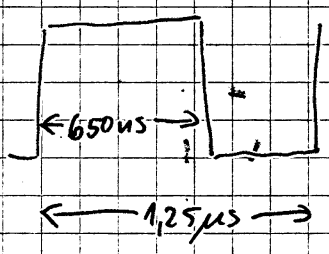




Lüfter:
Rotron Centaur CT3B79
115V 14W
Lochabstand 105 mm
Höhe 38 mm



CDD-Controller
(von Saloschin)



SCEIN

SCUZ	Bremen	72995
"	VA	68552
	Frewer	68553

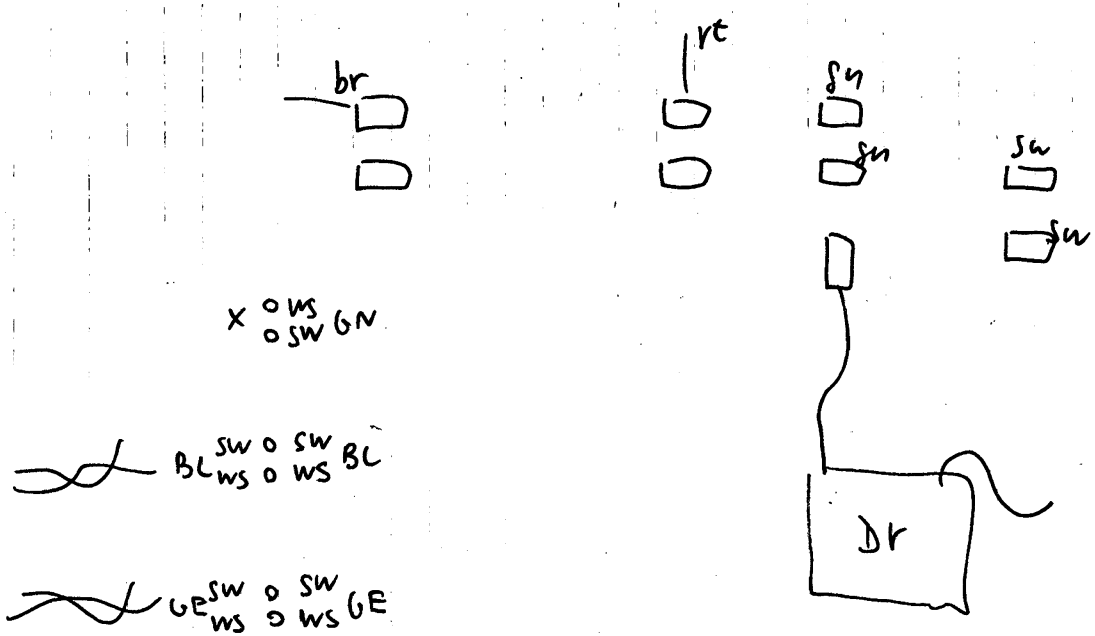
ASCU 68276

6400

SCUZ	68553
CPU	72983
SACUZ	66943
CRUPZ	70671

Marque	CIMEA
Type	Multisource
Réf	TRE2
N° de Série	TA 1105
Primaires	100V / 5,4A
	115V / 4,7A
	220V / 2,2A
	240V / 2A
Fréqu.	50Hz / 60Hz
Puissance	600VA

E2
Mains Transformer


br
rt
sw
sw
sw
sw
X
ws
sw
GN
BL
sw
sw
ws
ws
BL
GE
sw
sw
ws
ws
GE
Dr

5111 199 77302 #133

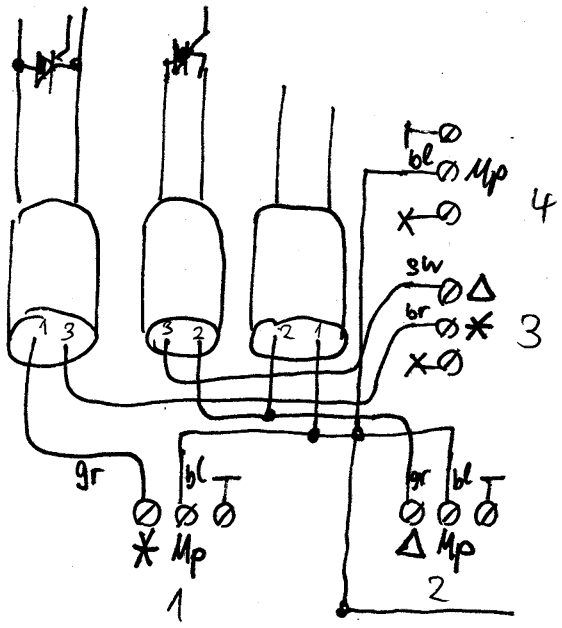
chassis	~~80~~	7840 2 (vom)	7842 2 (hinten) – RACK7-133
Support		7837 2	
PMPU7		2871 1	#115
BPU7		7828 5	#1330
C.IMP		7830-1	#147
ENS.PC		7833 2	#153
OSB1		7831	154

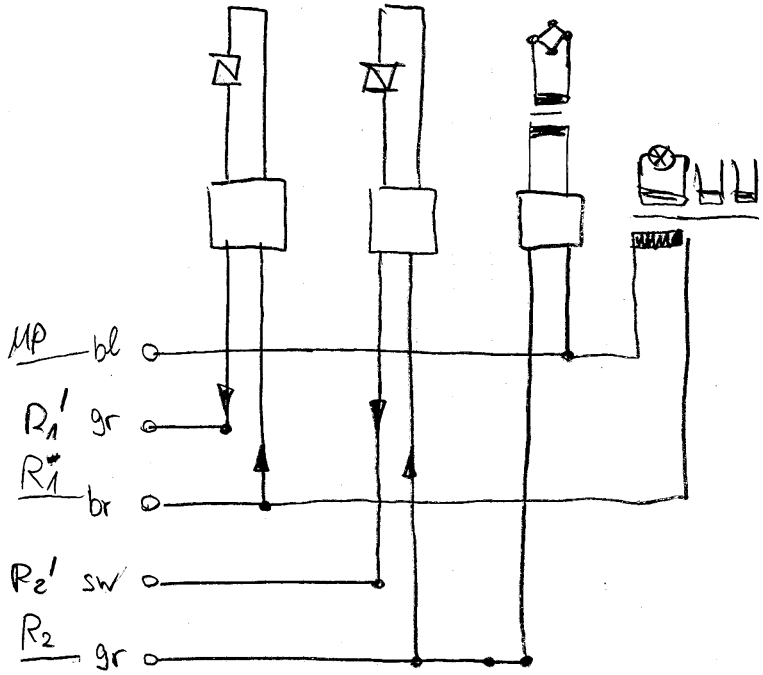
				Mechanics
Drive 2	PC 1580/00 = 9406 215 80001	D719		2576
1		D724		2501
0		D725		2397

5111 199 7817 -

3 → 4	M	accidental sector destruction	2613-16-003
4 → 6 5 → 6	M	Interrupt from 2 drives / Restart of UNSAFE / timing with IOC2-PS1	2613-16-005
—		checks component location error	P24C002
6 → 7	M	incorrect length	P24C006
7 → 8	R	Read error on high temperature	007

C 302
= PE 1279

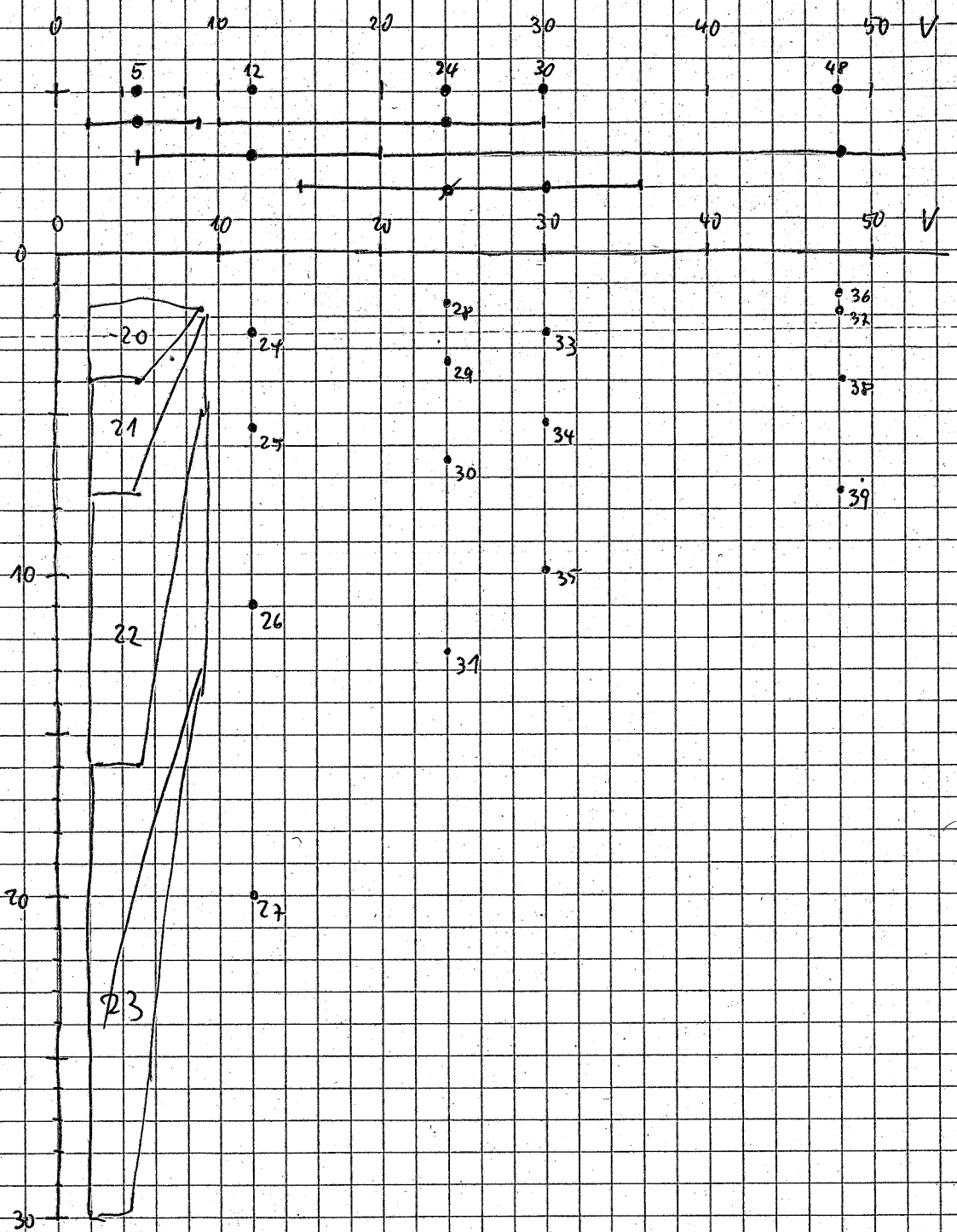




GAS ANZEIGER

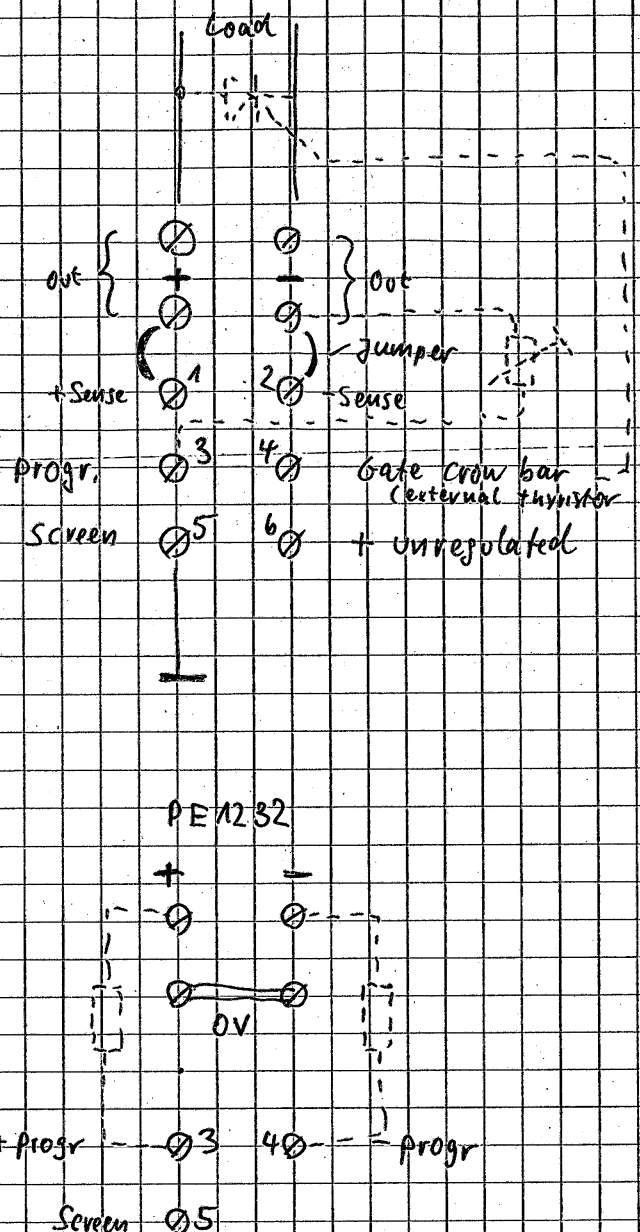
PE 1279

PE 12-



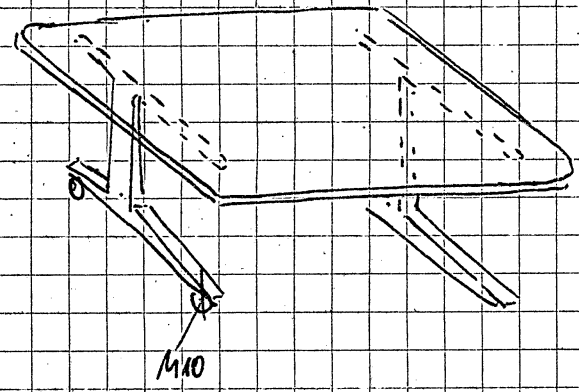
A
bei 55°

PE 12XX


Load
out
+
−
out
jumper
+Sense
1
2
Sense
progr.
3
4
Gate crow bar
(external thyristor
Screen
5
6
+ unregolated
PE1232
+
−
0V
+progr
3
4
progr
Screen
5

PE 12XX

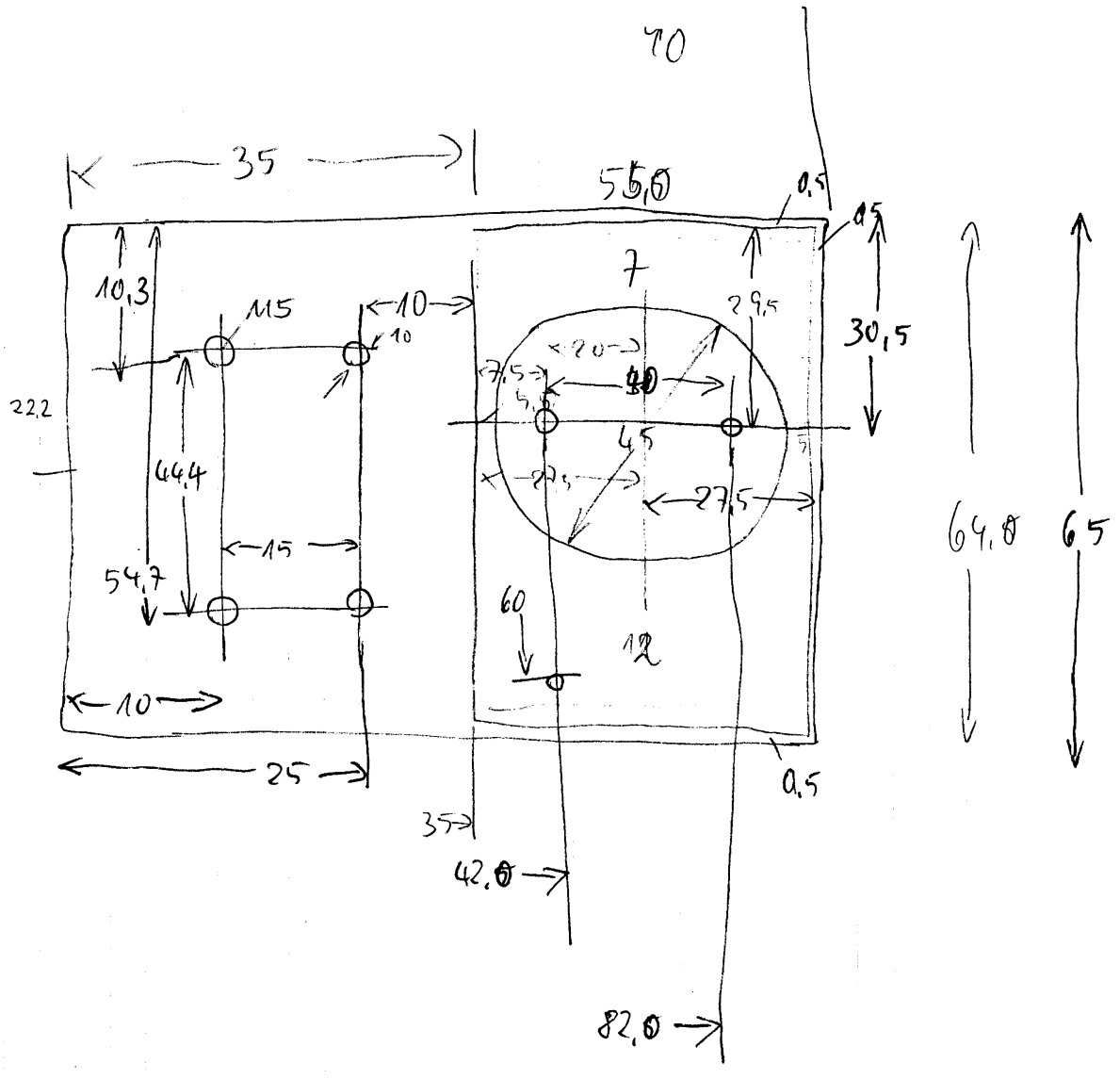




70,0
50,6

140,0
112,5
27,5 : 2 = 13,75

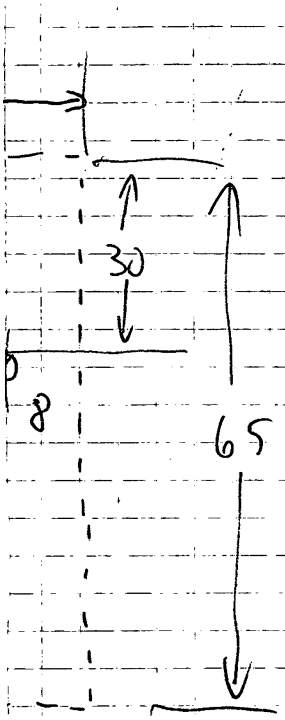
Terminal Table

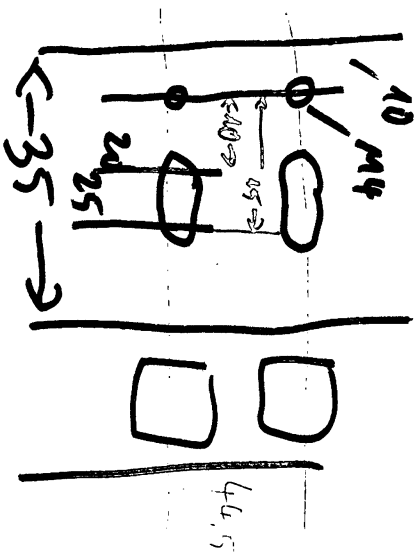


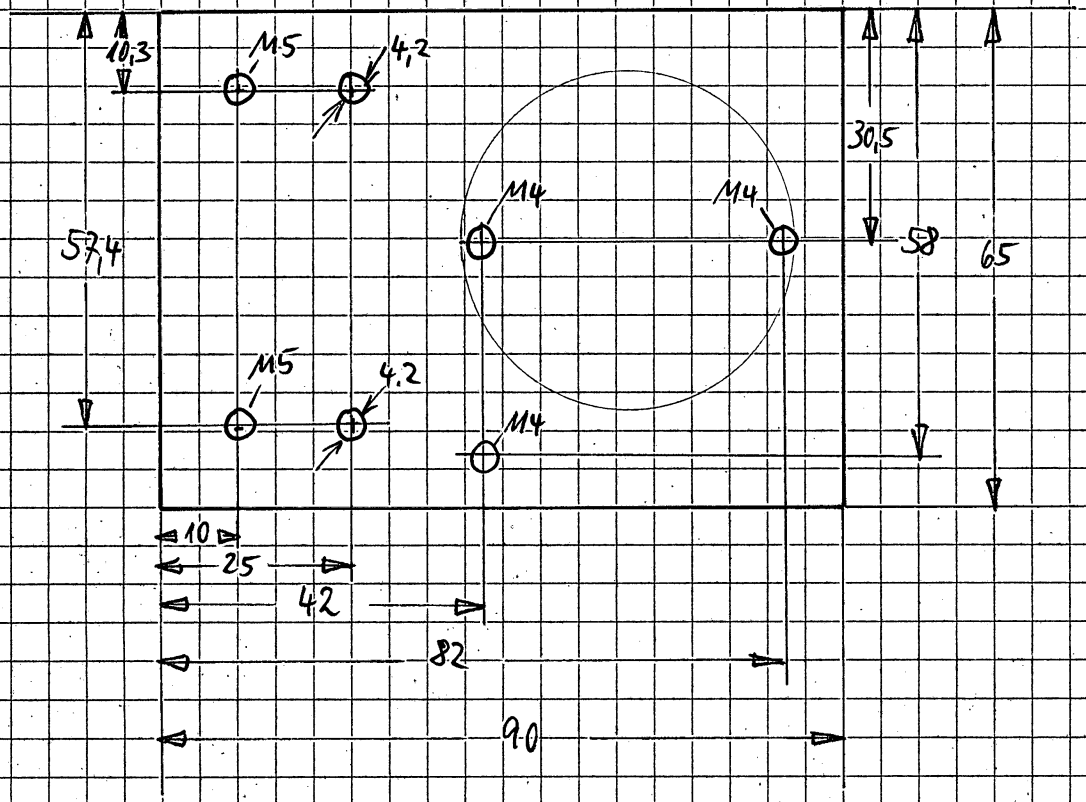
70
35
55,0
0,5
0,5
10,3
M5
10
10
7
29,5
30,5
20
7,5
40
5,5
45
22,2
44,4
27,5
27,5
15
54,7
60
12
64,0
65
10
25
0,5
35
42,0
82,0

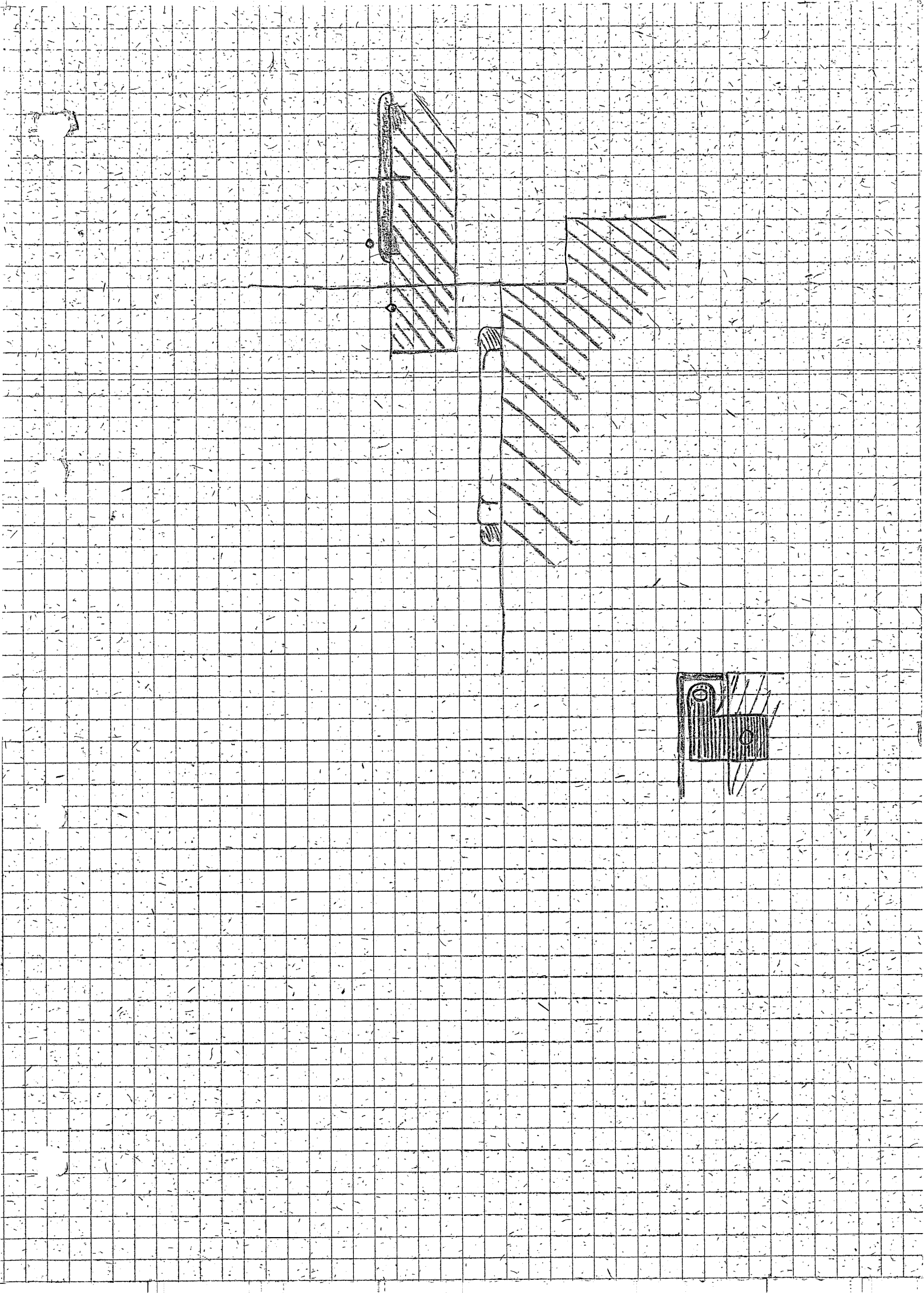
pon outlet

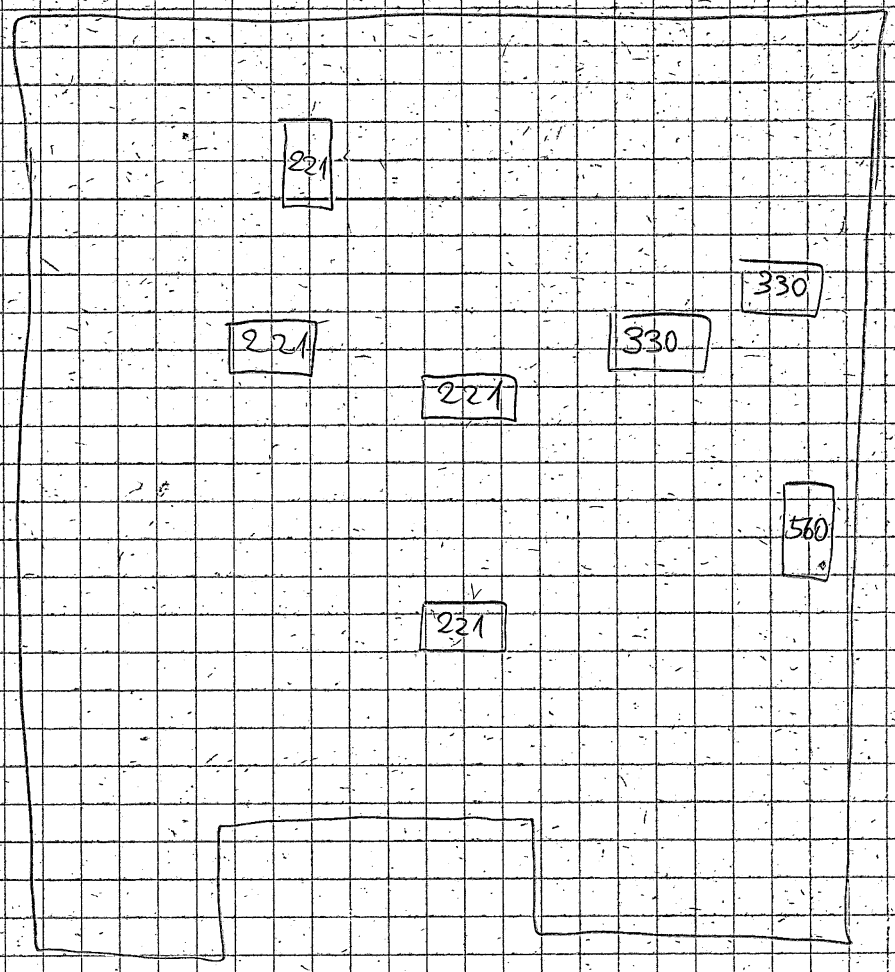
Bier
Cidre herb





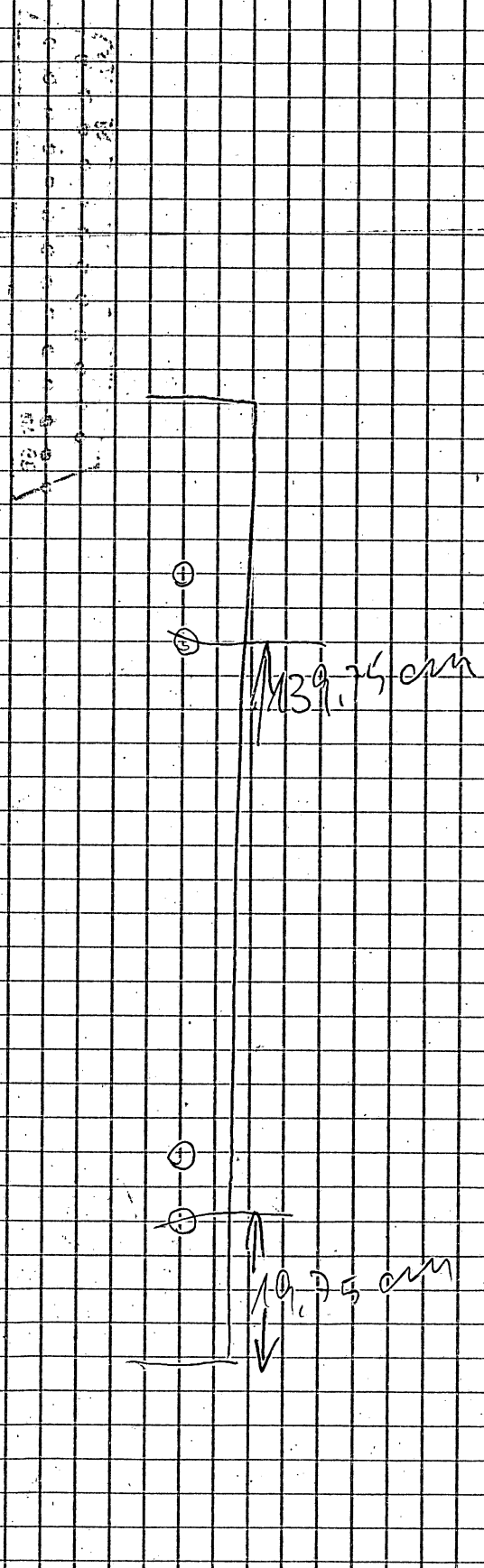

10,3
M5
4,2
57,4
M5
4.2
M4
M4
M4
30,5
58
65
10
25
42
82
90





4 x 220p
2 x 330p
1 x 560p

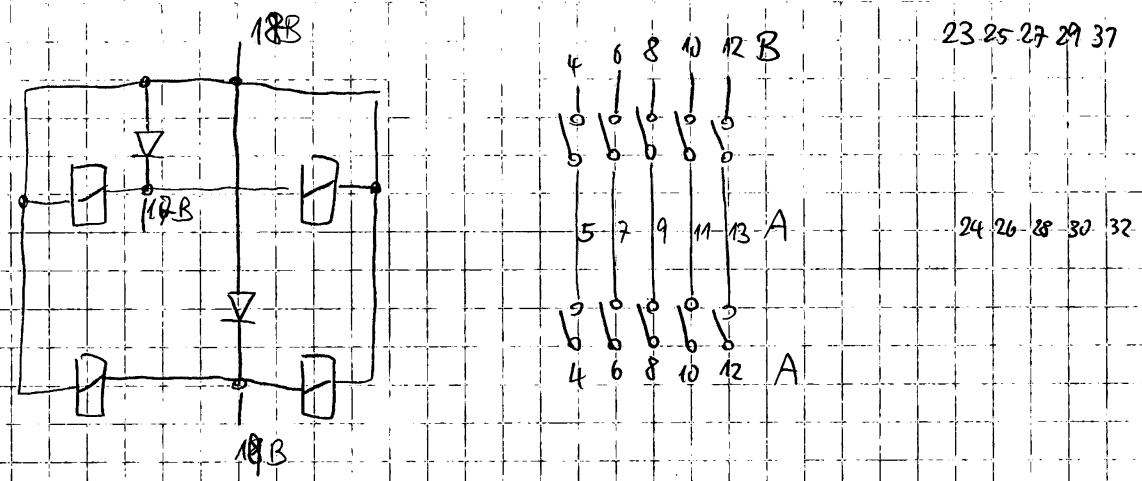
RM 7,5 mm


1
2
139,75 cm
1
2
19,75 cm

1	Memorex	Mark III 2T24	DD	B409774	24	B
2	"	"	"	B419931	24	B
3		"		B434024	24	B
4	—	CSCD 195		W004425	24	B
5	—	"		W004414		B
6	PDS (BASF)			C0400V		S
7				C9997V		S
8				C0285V		S
9				C0305V		S
10				C0253V		S
11	BASF			~~C-5280-V~~ C0428B		B
12				~~C0428B~~ C5280V		B
13				C9475P		S
~~14~~				C9662V		S
~~15~~				C9476P		S
16				C5281V		S
17				C8790V		S
18				C9468P		S
19				C8785V		S
20				C8932V		S

2.

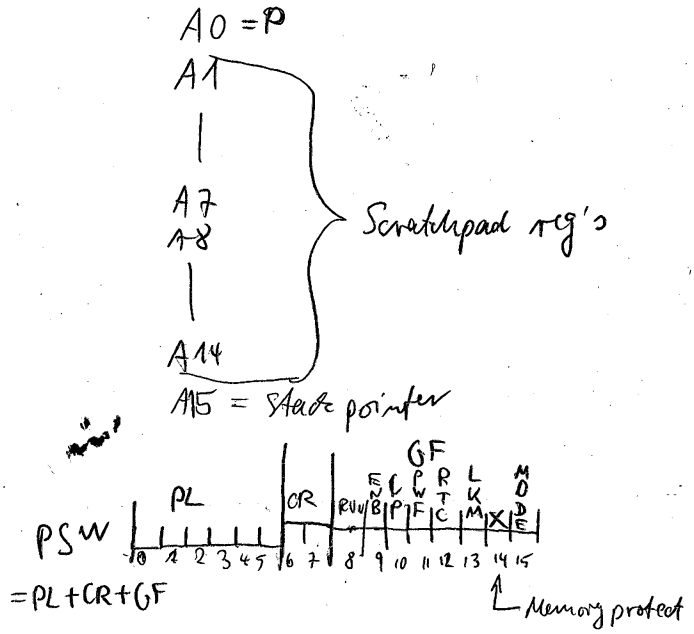
24-Slot Disk Cartridges



P-1400 SESSL

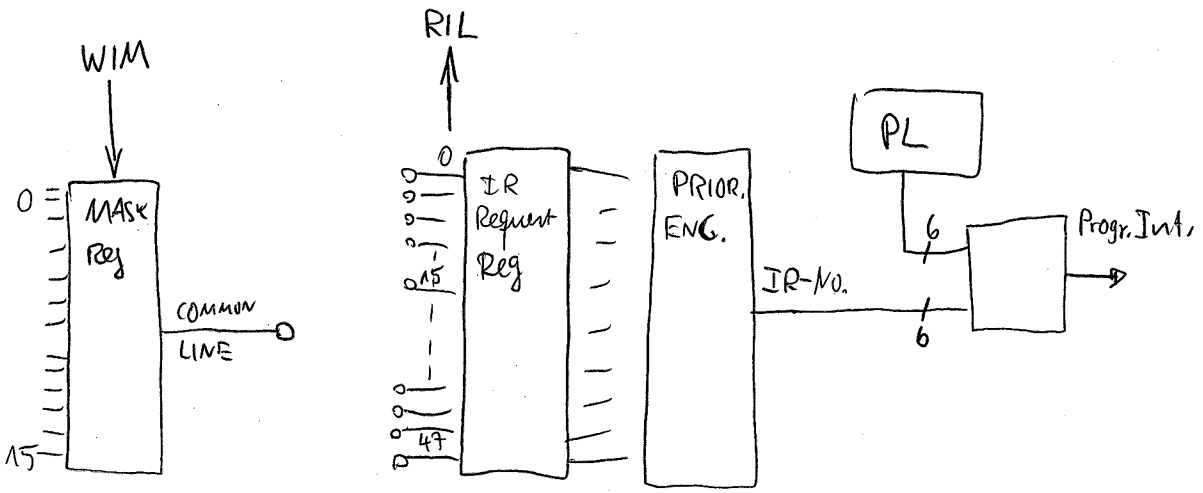
Relaisfante

P800 M Register



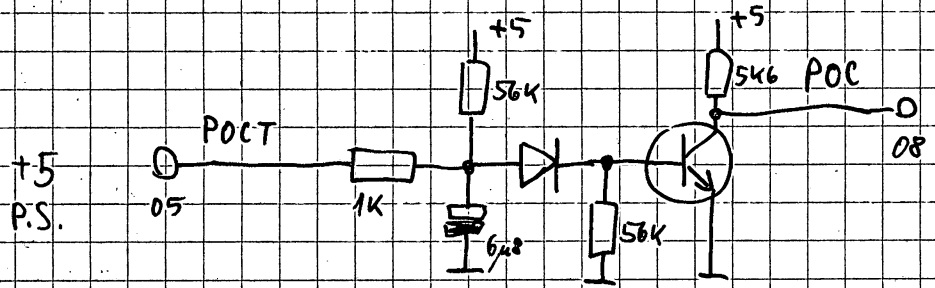
P855: IM Interrupt mask

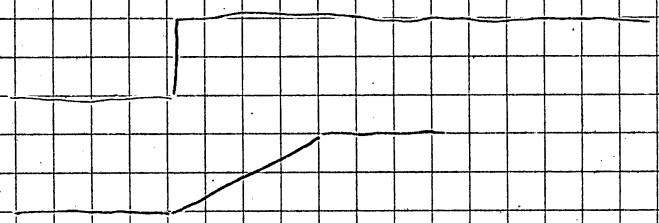
Write Interrupt Mask
Read Interrupt Lines



P800 Registers

P855 Interrupt





IG PA

56

Kugellager

interlace = 3

Phys	Log
0	0
1	11
2	6
3	1
4	12
5	7
6	2
7	13
8	8
9	3
10	14
11	9
12	4
13	15
14	10
15	5

Log	Phys	
0	0	VOLAB
1	3	IPL
2	6	Catalogue 1-PT DAD
3	9	
4	12	
5	15	
6	2	Bad track list
7	5	VTOC
8	8	
9	11	
10	14	
11	1	
12	4	
13	7	
14	10	
15	13	

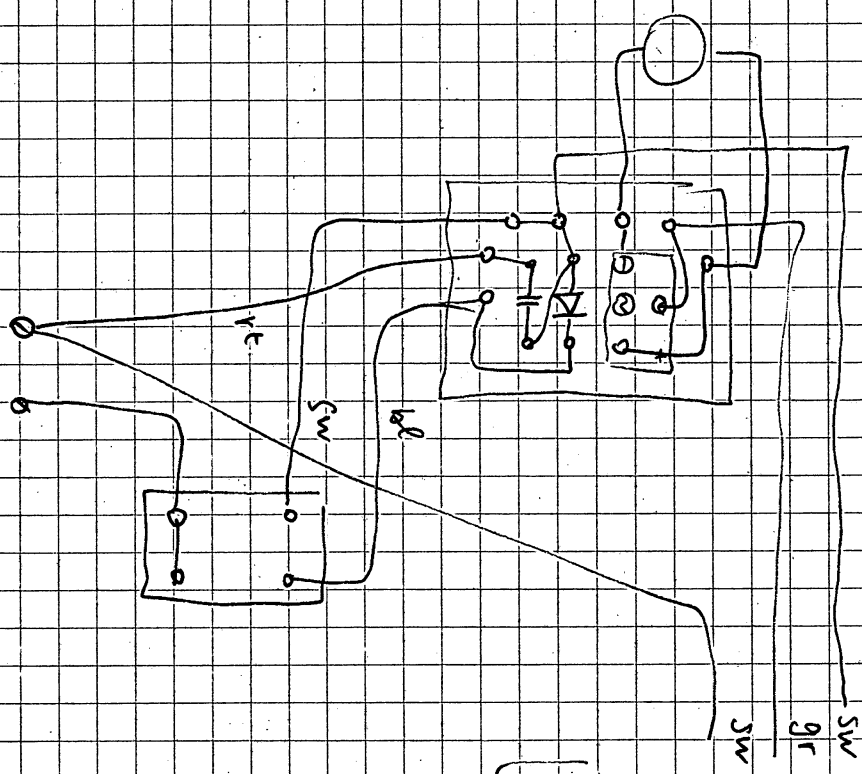
M1 3E

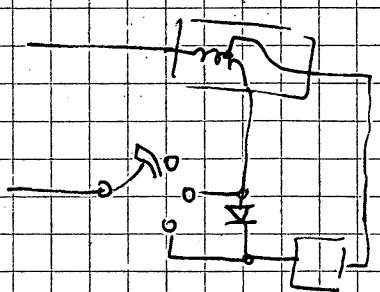
M2 3E E2

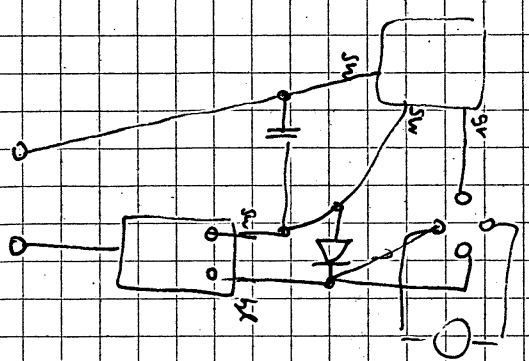
M3

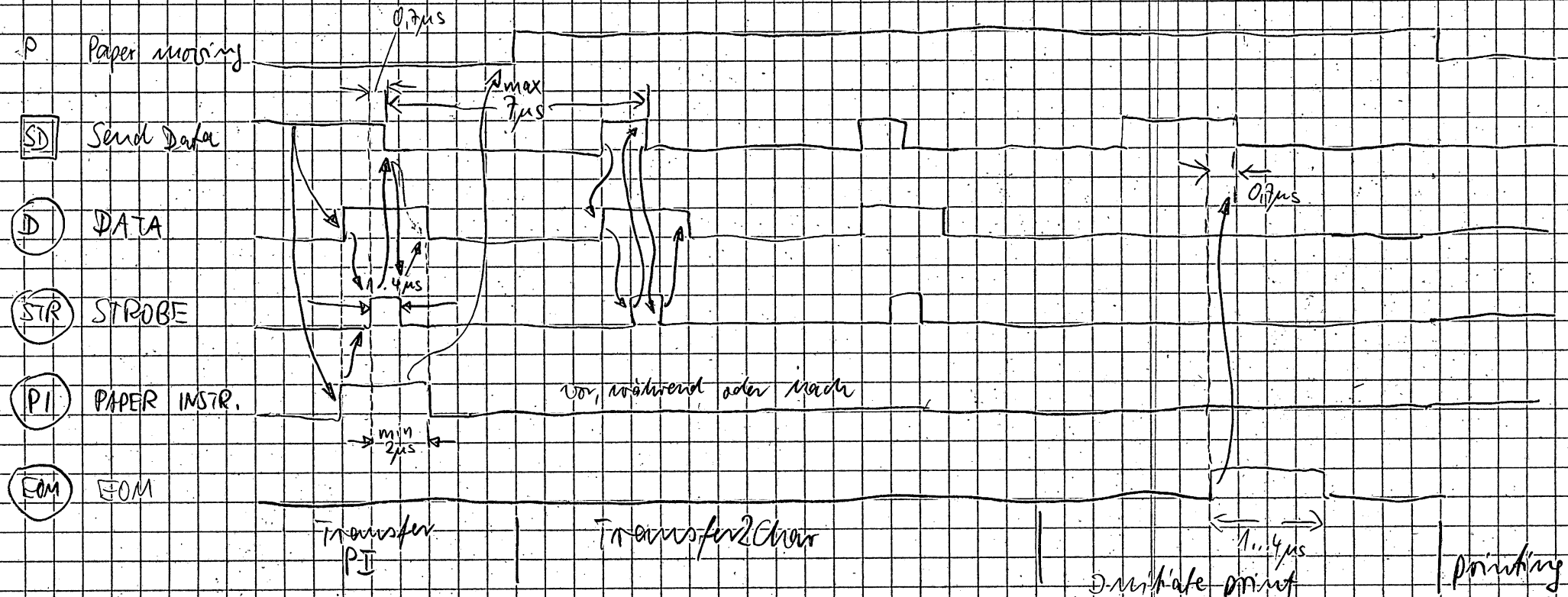
M4 = 6E

M5 = 11E

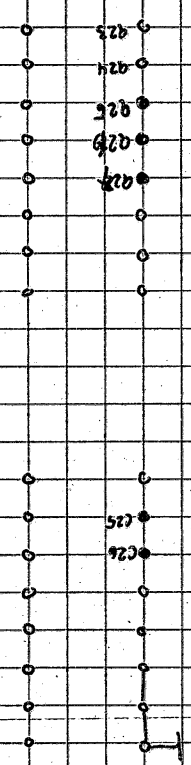








P880
Line printer



28,75
1,1,50
4025

Userid: diskFc: Dadname, userid

DCU <us1>
|
<userid>[, <das>]

<dim>[:DADname] | <dfc>
diskfile | dadfile
/Fx | /Cx

DCU Z80, /F1
BYE
Userid: /F1, Z80

SVU Z80, /F0: PROMSO

Blaupunkt
78107-1

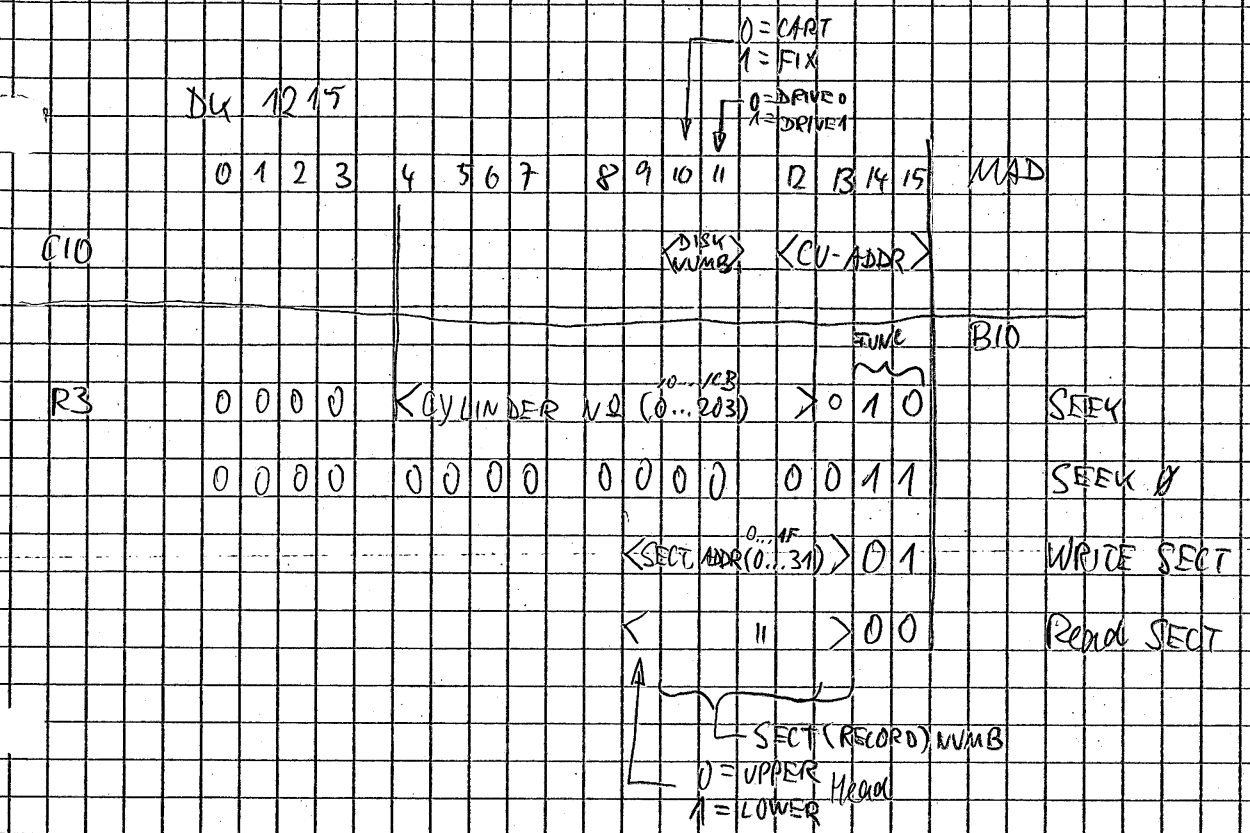
Passat 79 85 PS

742

A.H. Wevers WZH 6-24 209 TED, CIA

J Veldhuis WY 255 953 TED

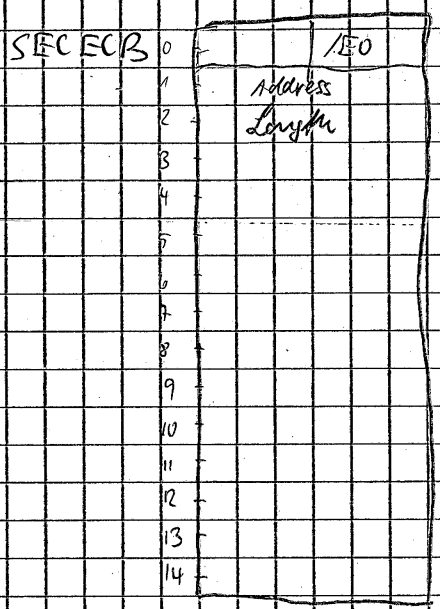
Peter Bijlsma

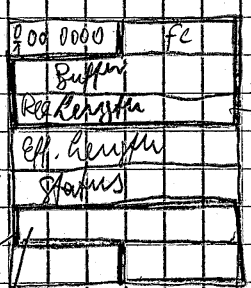

0 = CART
1 = FIX
0 = DRIVE 0
1 = DRIVE 1
DL 12 15
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
MAD
C10
DISK NUMB
CU-ADDR
FUNC
B10
R3
0 0 0 0
CYLINDER NR (0...203)
0 1 0
SEEK
0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
SEEK H
SECT ADDR (0...1F 0...31)
0 1
WRITE SECT
11
0 0
Read SECT
SECT (RECORD) NUMB
0 = UPPER Head
1 = LOWER

EDISEC

1 1 1 0 | 0 0 0 0 = /E0

SECECB





0	/E0
1	Address
2	Length
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	

} MLK 3 / MS 3, SECECB

0	0 00 0000	fc
1	Buffer	
2	Rec Length	
3	Eff. Length	
4	Status	
5		
6		

X1215 : /19A = 410 byte

ignored by DOS

Data Floppy 1 sect = 128 byte
4 " = 512 "

1st Sector abs Addr.
(0 ... 2001)

1) rel. Sect. No (direct access file)
2) abs. " " (phys. access order /11 and /15)
3) Tabulator for TY

DKER <da> | <HW-Status> | <phys Sector> <head> <cylinder> |

Track

Example 0 2

always 0 for 2504 floppy

" " "

0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

← floppy

X1215

EDISEC

```
DUMPFC    EQU   2
WORLIN    EQU   -10          words/line
SECECB    RES   15  words
STATUS          3
DISC FC         2
CYL             2
SECT            2
LEN             2
WNR             2
NEW             2
NO              8
BUFF            4096
```

```
EDS       MCLK  3
          DATA  IEO, TEXT-2, 24
```

		Event	Fc	
0	0	'E'	0	
1	2	TEXT-2		buffer addr.
2	4	2	24	requ. length
3	6	eff length		
4	8	Status		
5	10	Sect. Nr.		

EDISEC

```
LD      A1, DISCFC
LDKL    A2, BUFF
LDKL    A3, 4096 — =1000
MS      3, SECECB

LD      A1, CYL
LD      A2, SECT
MS      2, SECECB+10
```

SECECB		
	DISKFC	0
+2	BUFF ADDR	1
+4	RQL=4096	2
+6	EFL	3
+8	STAT	4
+10	CYL	5
+12	Head + Sect.	6
+15		

EDISEC

0
```
********
********
********
********
********
********
********
********
********
```

3
```
HALLO WANNI$
HALLO WANNI$
```

7
```
U*U*U*
```

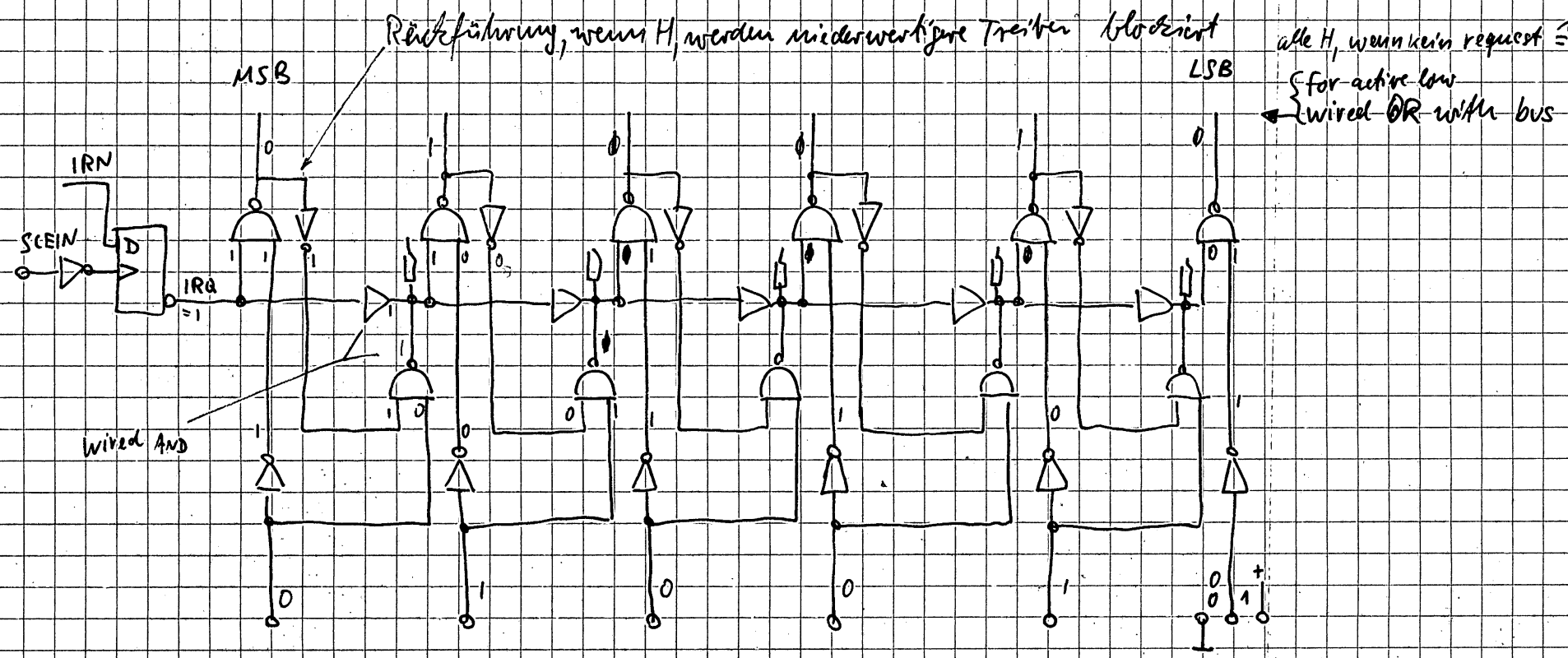
PROM

ADDR CODE

0000	0E	0D	0B	07	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
0010	0E	0E	0D	0D	0B	0B	07	07	0F	0F	0F	0F	0F	0F	0F	0F
0020	0E	0E	0E	0E	0D	0D	0D	0D	0B	0B	0B	0B	07	07	07	07
0030	0E	0D	0B	0F	0F	0F	07	07	0F	0F	0F	0F	0F	0F	0F	0F
0040	0E	0D	0F	0F	0B	0B	07	07	0F	0F	0F	0F	0F	0F	0F	0F
0050	0E	0F	0D	0D	0B	0B	07	07	0F	0F	0F	0F	0F	0F	0F	0F
0060	0E	0D	0B	0F	07	07	07	07	0F	0F	0F	0F	0F	0F	0F	0F
0070	0E	0D	0F	0F	0B	0B	0B	0B	07	07	07	07	0F	0F	0F	0F
0080	0E	0F	0F	0F	0D	0D	0D	0D	0B	0B	0B	0B	07	07	07	07
0090	0E	0F	0F	0F	0D	0D	0B	0B	07	07	07	07	0F	0F	0F	0F
00A0	0E	0F	0D	0D	0B	0B	0B	0B	07	07	07	07	0F	0F	0F	0F
00B0	0E	0E	0D	0B	07	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
00C0	0E	0E	0E	0E	0D	0B	07	0F	0F	0F	0F	0F	0F	0F	0F	0F
00D0	0E	0E	0D	0D	0B	07	0F	0F	0F	0F	0F	0F	0F	0D	0F	0F
00E0	0E	0E	0E	0E	0D	0D	0D	0D	0B	07	0F	0F	0F	0F	0F	0F
00F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F

T=

ELAPSED TIME =001999 PRINTED RECORDS =000116 PUNCHED RECORDS =000000
ASG FCOD=2,DVCE=DY2F



Belier
Interrupt Enc

RUN PREMDK,0

INITIALIZATION OF PREMARK
COMPLETE PREMARK: <return=yes> ←
DISK TYPE: <type> X1
LABEL: <16char.> LABEL (z.B.: VAHUFTEN)
DATE: <yy mm dd> 83 10 24
PACK NBR: <4char> 1234
DISK UNIT PHYSICAL ADDRESS: <HexHex> 22
DAD NAME: <6char> DOSDRM
NUMBER OF CYL OF <dadname>: <dec dec dec dec> 200
NUMBER OF INT OF < " >: <dec dec dec dec> 3
SYST. USERID: <8char.> SYSTEM
ANOTHER DAD: <OK|NO> NO

must be 0

NUMBER OF DEFECTIVE TRACKS: <number>

CU-Type

type	X1	X1215 with DAD				
	X2	X1216 " "				
	D1	40M				
	D2	80M				
	F1	Floppy	1/4M	system		
	2	"	1/4M	data		
	3	"	1M	System, DAD		
	4	"	1M	data	Form 2	(double head, double dens, 8 sect, 1,2M)
	5	"	1M	data	Form 1	(double head, double dens 26 sect, 1M)
	6	"	1M	data	Form 0	(single head, single dens/1/4M)
	M1	Mini-Fixed X1250, DAD				
	Vn	Fixed Head, DAD (n=1...8)				

		Exp	Actual
A	loops/Sec	1000	505
Br			1010
DC			1010

8S1-CPU
MMSYSTEST

```
7A   SST  A7,0
7C   RB(NA)   *-2
```

A15 63C2

A6 0081

A7 enthält 0

A4 " 7A

7A " 4FC2

~~8 9 10 11 12 13 14 15~~

OCOM

INT

M: <cmd> cmd = <char char> [␣,<par>{,|␣}<par>] [CR] LF

numeric always HEX without slash

ER cmd contains error, INT again

AS␣<fc>,<duda> [,<ln>[,{I|O}]]

DY on AM18 only

e.g. AS␣2,TY10 CR